MT6325 PMIC Datasheet

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Document Revision History

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1 Overview

1.1 Features

- Handles all 2G/3G/4G smart phone baseband power management
- Input range: 2.5 ~ 4.5V
- 8 buck converters and 28 LDOs optimized for specific 2G/3G/4G smart phone subsystems
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC.
- 32K RTC oscillator for system timing, 1.8 and 2.8V clock buffer output
- Flexibility for various configurations of indicator LED current source: 3 ISINK
- SPI interface
- Li-ion battery charging function
- USB Battery Charging Specification ver 1.1/1.2 (BC1.x) Compliance
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog reset
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge
- 244-pin VFBGA package

1.2 Applications

MT6325 is ideal for power management of 2G, 3G and 4G smart phones and other portable systems.

1.3 General Descriptions

MT6325 is a power management system chip optimized for 2G/3G/4G handsets and smart phones, containing 8 buck converters and 28 LDOs optimized for specific 2G/3G/4G smart phone subsystems.

LED drivers support up to 3 channels of LEDs with independent control. Flexible control includes register mode, PWM mode and breath mode.

Sophisticated controls are available for power-up, battery charging and the RTC alarm. MT6325 is optimized for maximum battery life, allowing the RTC circuit to stay alive without a battery for several hours.

MT6325 adopts SPI interface and 2 SRCLKEN control pins to control buck converters, LDOs, and various drivers; it provides enhanced safety control and protocol for handshaking with BB.

MT6325 is available in a 244-pin VFBGA package. The operating temperature ranges from -25 to +65°C.

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1.4 Ordering Information

Order #	Marking	Temp. range	Package
MT6325V/A		-25 ~ +65°C	VFBGA 244L

1.5 Top Marking Definition

MT6325V/A

YYWW: Date code

$: Random code

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1.6 Pin Assignments and Descriptions

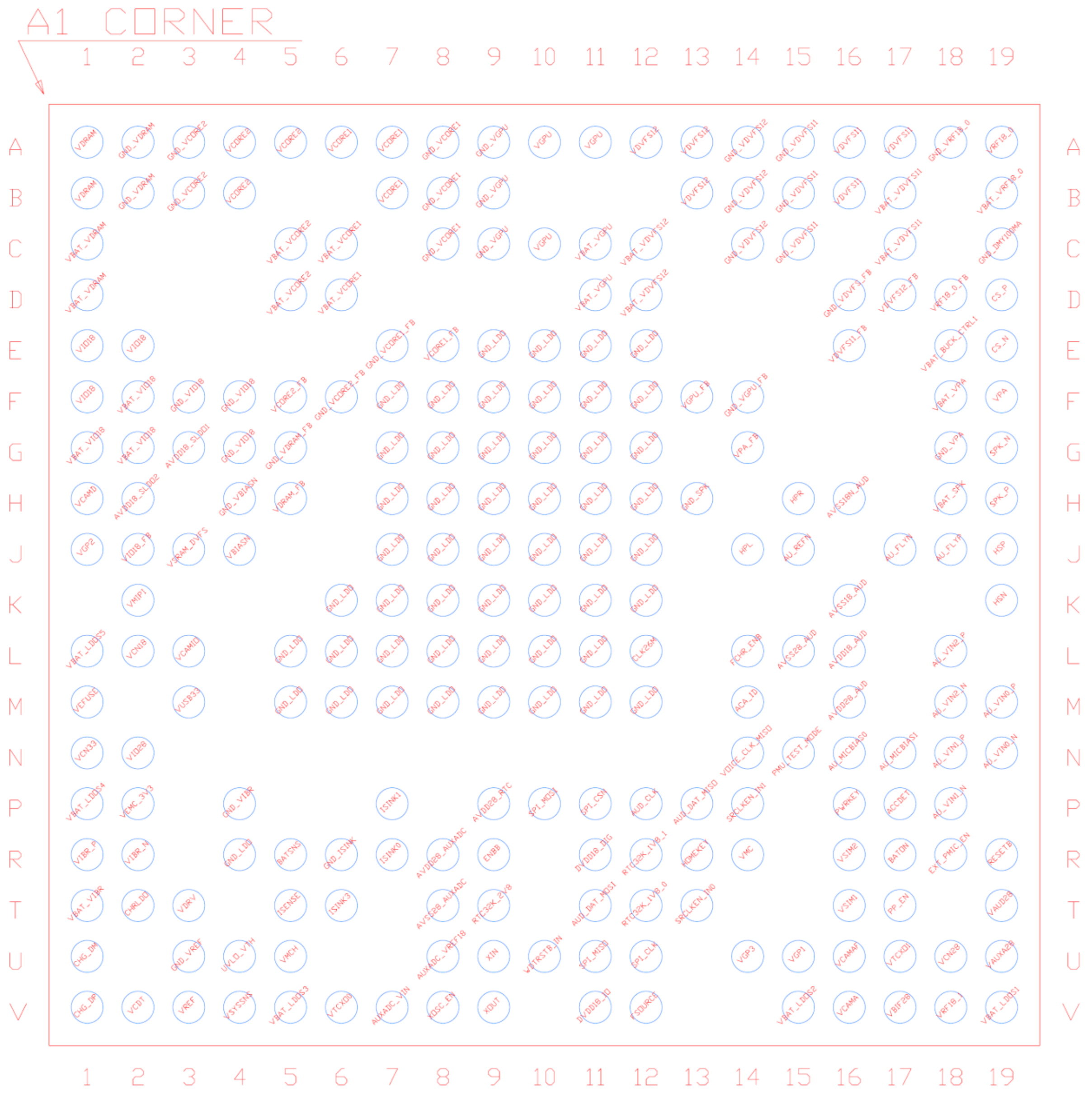

Figure 1-1. MT6325 VFBGA 244 (7.4x7.8mm) pin assignment

Table 1-1. MT6325 pin descriptions

Ball	Symbol	I/O	Description
M14	ACA_ID	I	BC1.2 ACA detection pin
P17	ACCDET	I	Accessory detection input
J17	AU_FLYN	O	Flying capacitor bottom
J18	AU_FLYP	O	Flying capacitor top
N16	AU_MICBIAS0	O	Microphone Bias 0

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Ball	Symbol	I/O	Description
N17	AU_MICBIAS1	O	Microphone Bias 1
J15	AU_REFN	GND	Audio reference ground
N19	AU_VIN0_N	I	Microphone channel 0 negative input
M19	AU_VIN0_P	I	Microphone channel 0 positive input
P18	AU_VIN1_N	I	Microphone channel 1 negative input
N18	AU_VIN1_P	I	Microphone channel 1 positive input
M18	AU_VIN2_N	I	Microphone channel 2 negative input
L18	AU_VIN2_P	I	Microphone channel 2 positive input
P12	AUD_CLK	I	Audio control interface
P13	AUD_DAT_MISO	IO	Audio control interface
T11	AUD_DAT_MOSI	IO	Audio control interface
V7	AUXADC_VIN	I	AUXADC input
U8	AUXADC_VREF18	O	1.8V AUXADC reference output
L16	AVDD18_AUD	PWR	1.8V power supply of Audio
G3	AVDD18_SLDO1	PWR	1.8V power supply of SLDO1
H2	AVDD18_SLDO2	PWR	1.8V power supply of SLDO2
M16	AVDD28_AUD	PWR	2.8V supply of Audio UL
R8	AVDD28_AUXADC	PWR	2.8V power supply of AUXADC
P9	AVDD28_RTC	O	RTC LDO output. Supply of RTC macro where backup battery can be added.
K16	AVSS18_AUD	GND	Audio DL ground
H16	AVSS18N_AUD	PWR	Audio -1.8V supply
L15	AVSS28_AUD	GND	Audio UL ground
T8	AVSS28_AUXADC	GND	AUXADC ground
R17	BATON	I	Battery NTC pin for battery and its temperature sensing
R5	BATSNS	I	Negative terminal for battery's charging current sensing resistor
U1	CHG_DM	I	USB D- for BC1.x standard
V1	CHG_DP	I	USB D+ for BC1.x standard
T2	CHRLDO	O	CHRLDO output voltage
L12	CLK26M	I	26MHz clock input
E19	CS_N	I	Fuel gauge ADC input pin
D19	CS_P	I	Fuel gauge ADC input pin
R11	DVDD18_DIG	O	VDIG18 output voltage
V11	DVDD18_IO	PWR	Digital IO power
R9	ENBB	O	ENBB control of RF chip
R18	EXT_PMIC_EN	IO	Ext chip MT6311/MT6312 enable pin
L14	FCHR_ENB	I	Force charging disable pin
V12	FSOURCE	PWR	EFUSE power source
C19	GND_DMY100MA	GND	GND for 100mA dummy load
R6	GND_ISINK	GND	ISINK ground
E9, E10, E11, E12, F7, F8, F9, F10, F11, F12, G7, G8, G9, G10, G11, G12, H7, H8, H9, H10, H11,	GND_LDO	GND	LDO ground

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Ball	Symbol	I/O	Description
H12, J7, J8, J9, J10, J11, J12, K6, K7, K8, K9, K10, K11, K12, L5, L6, L7, L8, L9, L10, L11, M5, M6, M7, M8, M9, M10, M11, M12, R4,			
H13	GND_SPK	GND	GND of internal speaker amp
H4	GND_VBIASN	GND	VBIASN ground
A8, B8, C8	GND_VCORE1	GND	VCORE1 ground
E7	GND_VCORE1_FB	I	Remote sense on ground of VCORE1
A3, B3	GND_VCORE2	GND	VCORE2 ground
F6	GND_VCORE2_FB	I	Remote sense on ground of VCORE2
A2, B2	GND_VDRAM	GND	VDRAM ground
G5	GND_VDRAM_FB	I	Remote sense on ground of VDRAM
D16	GND_VDVFS_FB	I	Remote sense on ground of VDVFS
A15, B15, C15	GND_VDVFS11	GND	VDVFS11 ground
A14, B14, C14	GND_VDVFS12	GND	VDVFS12 ground
A9, B9, C9	GND_VGPU	GND	VGPU ground
F14	GND_VGPU_FB	I	Remote sense on ground of VGPU
P4	GND_VIBR	GND	VIBR ground
F3, F4, G4	GND_VIO18	GND	VIO18 ground
G18	GND_VPA	GND	VPA ground
U3	GND_VREF	GND	Ground for bandgap
A18	GND_VRF18_0	GND	VRF18_0 ground
R13	HOMEKEY	I	HOMEKEY button
J14	HPL	O	Earphone left channel output
H15	HPR	O	Earphone right channel output
K19	HSN	O	Handset negative output
J19	HSP	O	Handset positive output
T5	ISENSE	I	Positive terminal for battery's charging current sensing resistor
R7	ISINK0	IO	ISINK channel 0
P7	ISINK1	IO	ISINK channel 1
T6	ISINK3	IO	ISINK channel 3
N15	PMU_TEST_MODE	I	PMU test mode signal (tied to GND in normal operation)
T17	PP_EN	O	Power path enable
P16	PWRKEY	I	PWRKEY button
R19	RESETB	O	System reset release signal
T12	RTC32K_1V8_0	O	VIO18 domain 32kHz clock output
R12	RTC32K_1V8_1	O	VIO18 domain 32kHz clock output
T9	RTC32K_2V8	O	VRTC domain 32kHz clock output
U12	SPI_CLK	I	SPI control interface
P11	SPI_CSN	IO	SPI control interface
U11	SPI_MISO	IO	SPI control interface
P10	SPI_MOSI	IO	SPI control interface

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Ball	Symbol	I/O	Description
G19	SPK_N	O	Negative output of internal speaker amp
H19	SPK_P	O	Positive output of internal speaker amp
T13	SRCLKEN_IN0	I	Source clock enable pin 0
P14	SRCLKEN_IN1	I	Source clock enable pin 1
U4	UVLO_VTH	I	UVLO threshold control pin
T19	VAUD28	O	VAUD28 output voltage
U19	VAUXA28	O	VAUXA28 output voltage
E18	VBAT_BUCK_CTRL1	PWR	Power supply of buck controller
V19	VBAT_LDOS1	PWR	Power supply input of LDO group1
V15	VBAT_LDOS2	PWR	Power supply input of LDO group2
V5	VBAT_LDOS3	PWR	Power supply input of LDO group3
P1	VBAT_LDOS4	PWR	Power supply input of LDO group4
L1	VBAT_LDOS5	PWR	Power supply input of LDO group5
H18	VBAT_SPK	PWR	Power supply of SPK
C6, D6	VBAT_VCORE1	PWR	Power supply of VCORE1
C5, D5	VBAT_VCORE2	PWR	Power supply of VCORE2
C1, D1	VBAT_VDRAM	PWR	Power supply of VDRAM
B17, C17	VBAT_VDVFS11	PWR	Power supply of VDVFS11
C12, D12	VBAT_VDVFS12	PWR	Power supply of VDVFS12
C11, D11	VBAT_VGPU	PWR	Power supply of VGPU
T1	VBAT_VIBR	PWR	Power supply input of Vibrator
F2, G1, G2	VBAT_VIO18	PWR	Power supply of VIO18
F18	VBAT_VPA	PWR	Power supply of VPA
B19	VBAT_VRF18_0	PWR	Power supply of VRF18_0
J4	VBIASN	O	VBIASN output voltage
V17	VBIF28	O	VBIF28 output voltage
V16	VCAMA	O	VCAMA output voltage
U16	VCAMAF	O	VCAMAF output voltage
H1	VCAMD	O	VCAMD output voltage
L3	VCAMIO	O	VCAMIO output voltage
V2	VCDT	I	Fractional charger input voltage for charger detection
L2	VCN18	O	VCN18 output voltage
U18	VCN28	O	VCN28 output voltage
N1	VCN33	O	VCN33 output voltage
A6, A7, B7	VCORE1	O	SW node of VCORE1
E8	VCORE1_FB	I	BUCK VCORE1 feedback pin
A4, A5, B4	VCORE2	O	SW node of VCORE2
F5	VCORE2_FB	I	BUCK VCORE2 feedback pin
A1, B1	VDRAM	O	SW node of VDRAM
H5	VDRAM_FB	I	BUCK VDRAM feedback pin
T3	VDRV	O	Charger current drive output
A16, A17, B16	VDVFS11	O	SW node of VDVFS11
E16	VDVFS11_FB	I	BUCK VDVFS11 feedback pin
A12, A13, B13	VDVFS12	O	SW node of VDVFS12

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Ball	Symbol	I/O	Description
D17	VDVFS12_FB	I	BUCK VDVFS12 feedback pin
M1	VEFUSE	O	VEFUSE output voltage
P2	VEMC_3V3	O	VEMC_3V3 output voltage
U15	VGP1	O	VGP1 output voltage
J1	VGP2	O	VGP2 output voltage
U14	VGP3	O	VGP3 output voltage
A10, A11, C10	VGPU	O	SW node of VGPU
F13	VGPU_FB	I	BUCK VGPU feedback pin
R2	VIBR_N	O	Negative output of VIBR
R1	VIBR_P	O	Positive output of VIBR
E1, E2, F1	VIO18	O	SW node of VIO18
J2	VIO18_FB	I	BUCK VIO18 feedback pin
N2	VIO28	O	VIO28 output voltage
R14	VMC	O	VMC output voltage
U5	VMCH	O	VMCH output voltage
K2	VMIPI	O	VMIPI output voltage
N14	VOICE_CLK_MISO	IO	Voice wakeup control pin
F19	VPA	O	SW node of VPA
G14	VPA_FB	I	BUCK VPA feedback pin
V3	VREF	O	Bandgap reference voltage
A19	VRF18_0	O	SW node of VRF18_0
D18	VRF18_0_FB	I	BUCK VRF18_0 feedback pin
V18	VRF18_1	O	VRF18_1 output voltage
T16	VSIM1	O	VSIM1 output voltage
R16	VSIM2	O	VSIM2 output voltage
J3	VSRAM_DVFS	O	VSRAM_DVFS output voltage
V4	VSYSSNS	PWR	VSYS supply input for internal block and UVLO detection
V6	VTCXO0	O	VTCXO0 output voltage
U17	VTCXO1	O	VTCXO1 output voltage
M3	VUSB33	O	VUSB33 output voltage
U10	WDTRSTB_IN	I	Watchdog reset from AP
U9	XIN	IO	32K crystal connection port while using crystal to generate 32kHz clock
V8	XOSC_EN	O	XOSC_EN control of RF chip
V9	XOUT	IO	32K crystal connection port while using crystal to generate 32kHz clock

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2 Electrical Characteristics

2.1 Absolute Maximum Ratings over Operating Free-Air Temperature Range

Stresses beyond those listed in Table 2-1. Absolute maximum ratings may cause permanent damage to the device. These numbers are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 2-1. Absolute maximum ratings

Parameter	Conditions	Min.	Typical	Max.	Unit
Free-air temperature range		-40		85	°C
Storage temperature range		-65		150	°C
Battery Pin input voltage range				4.5	V
ESD robustness	HBM	2,000			V
Charger input withstand				30	V

2.2 Thermal Characteristic

Parameter	Conditions	Min.	Typical	Max.	Unit
Thermal resistance from junction to ambient	In free air		51.87[1]		°C/W

Note: The device is mounted on a 4-metal-layer PCB and modeled per JEDEC51-9 condition.

2.3 Pin Voltage Range

The table below lists operation rang voltages for all MT6325 I/O pins.

Table 2-2. Pin voltage range

Ball	Symbol	Voltage range	Unit
M14	ACA_ID	0 ~ 3.3	v
P17	ACCDET	0 ~ 3.08	v
J17	AU_FLYN	-1.98 ~ 0	v
J18	AU_FLYP	0 ~ 1.8	v
N16	AU_MICBIAS0	0~3.08	v
N17	AU_MICBIAS1	0~3.08	v

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Ball	Symbol	Voltage range	Unit
J15	AU_REFN	0	v
N19	AU_VIN0_N	0~3.08	v
M19	AU_VIN0_P	0 ~ 3.08	v
P18	AU_VIN1_N	0 ~ 3.08	v
N18	AU_VIN1_P	0~3.08	v
M18	AU_VIN2_N	0 ~ 3.08	v
L18	AU_VIN2_P	0 ~ 3.08	v
P12	AUD_CLK	0 ~ 1.98	v
P13	AUD_DAT_MISO	0 ~ 1.98	v
T11	AUD_DAT_MOSI	0 ~ 1.98	v
V7	AUXADC_VIN	0 ~ 1.98	v
U8	AUXADC_VREF18	0 ~ 1.98	v
L16	AVDD18_AUD	0 ~ 1.98	v
G3	AVDD18_SLDO1	0 ~ 1.98	v
H2	AVDD18_SLDO2	0 ~ 1.98	v
M16	AVDD28_AUD	0 ~ 3.08	v
R8	AVDD28_AUXADC	0 ~ 3.08	v
P9	AVDD28_RTC	0~3.08	v
K16	AVSS18_AUD	0	v
H16	AVSS18N_AUD	-1.98 ~ 0	v
L15	AVSS28_AUD	0	v
T8	AVSS28_AUXADC	0	v
R17	BATON	0 ~ 4.5	v
R5	BATSNS	0 ~ 4.5	v
U1	CHG_DM	0 ~ 4.5	v
V1	CHG_DP	0 ~ 4.5	v
T2	CHRLDO	0 ~ 3.08	v
L12	CLK26M	0 ~ 1.98	v
E19	CS_N	0 ~ 0.1	v
D19	CS_P	0 ~ 0.1	v
R11	DVDD18_DIG	0 ~ 1.98	v
V11	DVDD18_IO	0 ~ 1.98	v
R9	ENBB	0 ~ 1.98	v
R18	EXT_PMIC_EN	0 ~ 4.5	v
L14	FCHR_ENB	0 ~ 4.5	v
V12	FSOURCE	0 ~ 1.98	v
C19	GND_DMY100MA	0	v

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Ball	Symbol	Voltage range	Unit
R6	GND_ISINK	0	V
E9, E10, E11, E12, F7, F8, F9, F10, F11, F12, G7, G8, G9, G10, G11, G12, H7, H8, H9, H10, H11, H12, J7, J8, J9, J10, J11, J12, K6, K7, K8, K9, K10, K11, K12, L5, L6, L7, L8, L9, L10, L11, M5, M6, M7, M8, M9, M10, M11, M12, R4,	GND_LDO	0	V
H13	GND_SPK	0	V
H4	GND_VBIASN	0	V
A8, B8, C8	GND_VCORE1	0	V
E7	GND_VCORE1_FB	0	V
A3, B3	GND_VCORE2	0	V
F6	GND_VCORE2_FB	0	V
A2, B2	GND_VDRAM	0	V
G5	GND_VDRAM_FB	0	V
D16	GND_VDVFS_FB	0	V
A15, B15, C15	GND_VDVFS11	0	V
A14, B14, C14	GND_VDVFS12	0	V
A9, B9, C9	GND_VGPU	0	V
F14	GND_VGPU_FB	0	V
P4	GND_VIBR	0	V
F3, F4, G4	GND_VIO18	0	V
G18	GND_VPA	0	V
U3	GND_VREF	0	V
A18	GND_VRF18_0	0	V
R13	HOMEKEY	0 ~ 1.98	V
J14	HPL	-1.98 ~ 1.98	V
H15	HPR	-1.98 ~ 1.98	V
K19	HSN	-1.98 ~ 1.98	V
J19	HSP	-1.98 ~ 1.98	V
T5	ISENSE	0 ~ 4.5	V
R7	ISINK0	0 ~ 4.5	V
P7	ISINK1	0 ~ 4.5	V
T6	ISINK3	0 ~ 4.5	V
N15	PMU_TEST_MODE	0 ~ 4.5	V
T17	PP_EN	0 ~ 4.5	V
P16	PWRKEY	0 ~ 4.5	V
R19	RESETB	0 ~ 1.98	V

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Ball	Symbol	Voltage range	Unit
T12	RTC32K_1V8_0	0 ~ 1.98	V
R12	RTC32K_1V8_1	0 ~ 1.98	V
T9	RTC32K_2V8	0 ~ 3.08	V
U12	SPI_CLK	0 ~ 1.98	V
P11	SPI_CSN	0 ~ 1.98	V
U11	SPI_MISO	0 ~ 1.98	V
P10	SPI_MOSI	0 ~ 1.98	V
G19	SPK_N	0 ~ 4.5	V
H19	SPK_P	0 ~ 4.5	V
T13	SRCLKEN_IN0	0 ~ 1.98	V
P14	SRCLKEN_IN1	0 ~ 1.98	V
U4	UVLO_VTH	0 ~ 3.3	V
T19	VAUD28	0 ~ 4.5	V
U19	VAUXA28	0 ~ 4.5	V
E18	VBAT_BUCK_CTRL1	0 ~ 4.5	V
V19	VBAT_LDOS1	0 ~ 4.5	V
V15	VBAT_LDOS2	0 ~ 4.5	V
V5	VBAT_LDOS3	0 ~ 4.5	V
P1	VBAT_LDOS4	0 ~ 4.5	V
L1	VBAT_LDOS5	0 ~ 4.5	V
H18	VBAT_SPK	0 ~ 4.5	V
C6, D6	VBAT_VCORE1	0 ~ 4.5	V
C5, D5	VBAT_VCORE2	0 ~ 4.5	V
C1, D1	VBAT_VDRAM	0 ~ 4.5	V
B17, C17	VBAT_VDVFS11	0 ~ 4.5	V
C12, D12	VBAT_VDVFS12	0 ~ 4.5	V
C11, D11	VBAT_VGPU	0 ~ 4.5	V
T1	VBAT_VIBR	0 ~ 4.5	V
F2, G1, G2	VBAT_VIO18	0 ~ 4.5	V
F18	VBAT_VPA	0 ~ 4.5	V
B19	VBAT_VRF18_0	0 ~ 4.5	V
J4	VBIASN	0 ~ 0.8	V
V17	VBIF28	0 ~ 4.5	V
V16	VCAMA	0 ~ 4.5	V
U16	VCAMAF	0 ~ 4.5	V
H1	VCAMD	0 ~ 1.98	V
L3	VCAMIO	0 ~ 4.5	V

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Ball	Symbol	Voltage range	Unit
V2	VCDT	0 ~ 3.3	V
L2	VCN18	0 ~ 4.5	V
U18	VCN28	0 ~ 4.5	V
N1	VCN33	0 ~ 4.5	V
A6, A7, B7	VCORE1	0 ~ 4.5	V
E8	VCORE1_FB	0 ~ 4.5	V
A4, A5, B4	VCORE2	0 ~ 4.5	V
F5	VCORE2_FB	0 ~ 4.5	V
A1, B1	VDRAM	0 ~ 4.5	V
H5	VDRAM_FB	0 ~ 4.5	V
T3	VDRV	0 ~ 4.5	V
A16, A17, B16	VDVFS11	0 ~ 4.5	V
E16	VDVFS11_FB	0 ~ 4.5	V
A12, A13, B13	VDVFS12	0 ~ 4.5	V
D17	VDVFS12_FB	0 ~ 4.5	V
M1	VEFUSE	0 ~ 4.5	V
P2	VEMC_3V3	0 ~ 4.5	V
U15	VGP1	0 ~ 4.5	V
J1	VGP2	0 ~ 1.98	V
U14	VGP3	0 ~ 4.5	V
A10, A11, C10	VGPU	0 ~ 4.5	V
F13	VGPU_FB	0 ~ 4.5	V
R2	VIBR_N	0 ~ 3.3	V
R1	VIBR_P	0 ~ 3.3	V
E1, E2, F1	VIO18	0 ~ 4.5	V
J2	VIO18_FB	0 ~ 4.5	V
N2	VIO28	0 ~ 4.5	V
R14	VMC	0 ~ 4.5	V
U5	VMCH	0 ~ 4.5	V
K2	VMIPI	0 ~ 4.5	V
N14	VOICE_CLK_MISO	0 ~ 1.98	V
F19	VPA	0 ~ 4.5	V
G14	VPA_FB	0 ~ 4.5	V
V3	VREF	0 ~ 1.32	V
A19	VRF18_0	0 ~ 4.5	V
D18	VRF18_0_FB	0 ~ 4.5	V
V18	VRF18_1	0 ~ 4.5	V

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Ball	Symbol	Voltage range	Unit
T16	VSIM1	0 ~ 4.5	v
R16	VSIM2	0 ~ 4.5	v
J3	VSRAM_DVFS	0 ~ 1.98	v
V4	VSYSSNS	0 ~ 4.5	v
V6	VTCXO0	0 ~ 4.5	v
U17	VTCXO1	0 ~ 4.5	v
M3	VUSB33	0 ~ 4.5	v
U10	WDTRSTB_IN	0 ~ 1.98	v
U9	XIN	0 ~ 3.08	v
V8	XOSC_EN	0 ~ 3.08	v
V9	XOUT	0 ~ 3.08	v

2.4 Recommended Operating Range

Table 2-3. Operation condition

Parameter	Conditions	Min.	Typical	Max.	Unit
Operating temperature range		-25		65	°C

2.5 Electrical Characteristics

VBAT = 2.5 ~ 4.5V, minimum loads applied on all outputs, unless otherwise noted.
Typical values are at T_A = 25°C.

Table 2-4. General electrical specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Operation Ground Current					
Standby	Low-power mode		350		µA
Power down leakage current with 32K XTAL	VBAT=4.5V, Temp=-40℃~85℃		85	TBD	uA
Power down leakage current without 32K XTAL	VBAT=4.5V, Temp=-40℃~85℃		220	TBD	uA
Under Voltage (UV)					
Under voltage falling threshold 1	Programmable, 50mV steps.	2.5	2.6	2.9	V
Threshold voltage accuracy		-50		+50	mV
Under voltage rising threshold	UV_SEL[4:0] = xxxxx (w/o charger)	2.95	3.0	3.05	V
Under voltage rising threshold w/o power path	UV_SEL[4:0] = xxxxx (w/i charger)	2.75	2.8	2.85	V

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Parameter	Conditions	Min.	Typical	Max.	Unit
Under voltage rising threshold with power path	UV_SEL[4:0] = xxxxx (w/i charger)	2.95	3.0	3.05	V
Reset Generator					
Output high		VIO-0.4			V
Output low				0.2	V
Output current (Ioh)	Vo > VIO-0.4V		1		mA
Delay Time from VMC turn on to RESETB release		32	40	48	ms
Interrupt					
Output high		VIO-0.4			V
Output low				0.2	V
PWRKEY					
High voltage		0.7*VBAT			V
Low voltage				0.3*VBAT	V
De-bounce time		26	32	38	ms
Control Input Voltage					
Control input high (HOMEKEY, SPI, SRCLKEN related)		0.7*VIO			V
Control input low (HOMEKEY, SPI, SRCLKEN related)				0.3*VIO	V
Thermal Shut-down					
PMIC shut-down threshold			150		degree
Shut-down release threshold			110		degree

2.6 Regulator Output

Table 2-5. Buck specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Buck – VDVFS11/12					
Turn-on overshoot	No load			10	%
Short current		Imax*1.2		Imax*2.5	
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=0.8V, L_DCR=40mohm I_Load=100mA		81		%
	Vbat=3.8V, Vout=0.8V, L_DCR=40mohm I_Load=500mA		79		%
	Vbat=3.8V, Vout=1.0V, L_DCR=40mohm I_Load=2.5A		80		%
	Vbat=3.8V, Vout=1.1V, L_DCR=40mohm I_Load=4A		75		%
Soft start	No load			1	ms
Output Ripple Voltage (PWM)	Vbat=3.8V,			20	mVpp

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Parameter	Conditions	Min.	Typical	Max.	Unit
	I_Load=0.5*Imax 20MHz measurement BW				
Load transient(PWM)	Vbat=3.8V IOUT = 1.5A to 4A (slew rate=2.5A/us)	-3.5		+3.5	%
DC Accuracy (Included Line/Load regulation @PWM)	VBAT=2.8V to 4.5V I_Load=10mA to Imax	-1		+1	%
DC Accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.5V I_Load=0~10mA	-2		+3	%
Buck – VCORE1					
Turn-on overshoot	No load			10	%
Short current		Imax*1.2		Imax*2.5	
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=0.9V, L_DCR=40mohm I_Load=100mA		83		%
	Vbat=3.8V, Vout=1.0V, L_DCR=40mohm I_Load=800mA		82		%
	Vbat=3.8V, Vout=1.0V L_DCR=40mohm I_Load=1.5A		76		%
Soft start	No load			1	ms
Output Ripple Voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient(PWM)	Vbat=3.8V IOUT = 1.0A to 2.0A (slew rate=1A/us)	-3.5		+3.5	%
DC Accuracy (Included Line/Load regulation @PWM)	VBAT=2.8V to 4.5V I_Load=10mA to Imax	-1		+1	%
DC Accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.5V I_Load=0~10mA	-2		+3	%
Buck – VCORE2					
Turn-on overshoot	No load			10	%
Short current		Imax*1.2		Imax*2.5	
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=0.9V, L_DCR=40mohm I_Load=100mA		83		%
	Vbat=3.8V, Vout=1.0V, L_DCR=40mohm I_Load=800mA		82		%
	Vbat=3.8V, Vout=1.0V L_DCR=40mohm		76		%

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Parameter	Conditions	Min.	Typical	Max.	Unit
	I_Load=1.5A				
Soft start	No load			1	ms
Output Ripple Voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient(PWM)	Vbat=3.8V IOUT = 1.0A to 2.5A (slew rate=1.5A/us)	-3.5		+3.5	%
DC Accuracy (Included Line/Load regulation @PWM)	VBAT=2.8V to 4.5V I_Load=10mA to Imax	-1		+1	%
DC Accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.5V I_Load=0~10mA	-2		+3	%
Buck – VGPU					
Turn-on overshoot	No load			10	%
Short current		Imax*1.2		Imax*2.5	
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=0.9V, L_DCR=40mohm I_Load=100mA		83		%
	Vbat=3.8V, Vout=1.0V, L_DCR=40mohm I_Load=800mA		82		%
	Vbat=3.8V, Vout=1.0V L_DCR=40mohm I_Load=1.5A		76		%
Soft start	No load			1	ms
Output Ripple Voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient(PWM)	Vbat=3.8V IOUT = 1.0A to 3.0A (slew rate=2A/us)	-3.5		+3.5	%
DC Accuracy (Included Line/Load regulation @PWM)	VBAT=2.8V to 4.5V I_Load=10mA to Imax	-1		+1	%
DC Accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.5V I_Load=0~10mA	-2		+3	%
Buck – VIO18					
Turn-on overshoot	No load			10	%
Short current		Imax*1.2		Imax*3	
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, L_DCR=40mohm I_Load=50mA		82		%
	Vbat=3.8V, L_DCR=40mohm I_Load=500mA		82		%

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Parameter	Conditions	Min.	Typical	Max.	Unit
	Vbat=3.8V, L_DCR=40mohm I_Load=1000mA		75		%
Soft start	No load			1	ms
Output Ripple Voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient(PWM)	Vbat=3.8V IOUT = 1.0A to 2.0A (slew rate=40mA/us)	-3.5		+3.5	%
DC Accuracy (Included Line/Load regulation @PWM)	VBAT=2.8V to 4.5V I_Load=10mA to Imax	-1		+1	%
DC Accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.5V I_Load=0~10mA	-2		+3	%
Buck – VDRAM					
Turn-on overshoot	No load			10	%
Short current		Imax*1.2		Imax*2.5	
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, Vout=1.2V, L_DCR=40mohm I_Load=50mA		82		%
	Vbat=3.8V, Vout=1.2V, L_DCR=40mohm I_Load=200mA		83		%
	Vbat=3.8V, Vout=1.2V, L_DCR=40mohm I_Load=800mA		80		%
Soft start	No load			1	ms
Output Ripple Voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			20	mVpp
Load transient(PWM)	Vbat=3.8V IOUT = 1.0A to 2.0A (slew rate=1A/us)	-3.5		+3.5	%
DC Accuracy (Included Line/Load regulation @PWM)	VBAT=2.8V to 4.5V I_Load=10mA to Imax	-1		+1	%
DC Accuracy (Included Line/Load regulation @PFM)	VBAT=2.8V to 4.5V I_Load=0~10mA	-2		+3	%
Buck – VPA					
Turn-on overshoot	No load			10	%
Short current				Imax*5	
Temperature Coefficient	Vbat=3.8V I_Load=0.5*Imax Vo=1.8V	-100		+100	ppm/C
Efficiency	Vbat=3.8V, L_DCR=110 mohm		80		%

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Parameter	Conditions	Min.	Typical	Max.	Unit
	I_Load=80mA Vo=1.2V				
	Vbat=3.8V, L_DCR=100 mohm I_Load=180mA Vo=2.4V		89		%
	Vbat=3.8V, L_DCR=100mohm I_Load=280mA Vo=3.4V		92		%
Soft start	No load			200	ms
Output Ripple Voltage (PWM)	Vbat=3.8V Vo=1.8V I_Load=0.5*Imax 20MHz measurement BW			30	mVpp
DC Accuracy (Included Line/Load regulation @PWM)	VBAT=2.8V to 4.5V Vo=1.7V I_Load=10mA~360mA	-5		+5	%
No load quiescent current (PFM)	VBAT=3.8V Vo=0.5V I_Load=0A		150		%
Buck – VRF18_0					
Turn-on overshoot	No load			10	%
Short current		Imax*1.2		Imax*5	
Temperature coefficient	Vbat=3.8V I_Load=0.5*Imax	-100		+100	ppm/C
Efficiency	Vbat=3.8V, L_DCR=80 mohm I_Load=50mA		84		%
	Vbat=3.8V, L_DCR=80 mohm I_Load=250mA		90		%
	Vbat=3.8V, L_DCR=80 mohm I_Load=450mA		85		%
Soft start	No load			200	us
Output Ripple Voltage (PWM)	Vbat=3.8V, I_Load=0.5*Imax 20MHz measurement BW			25	mVpp
Load transient (PWM)	IOUT = 0.1A to 0.2A (slew rate=0.1A/us)	-2		+2	%
DC Accuracy (Included Line/ Load regulation @PWM)	VBAT=2.8V to 4.5V I_Load=10mA to Imax	-4		+4	%
DC Accuracy (Included Line/ Load regulation @PFM)	VBAT=2.8V to 4.5V I_Load=0~10mA	-4		+4	%
No load quiescent current (PFM)	VBAT=3.8V I_Load=0mA		110		uA

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Table 2-6. LDO specifications

Parameter	Type	Conditions	Min.	Typical	Max.	Unit
VBAT range	All LDOs	Vout ≧ 2.2	Vout +0.35		4.5	V
		Vout < 2.2	2.5		4.5	V
Dropout voltage	All LDOs				350	mV
Line/ Load regulation	VTCXO0, VTCXO1	1. Iout = 0~Imax 2. VBAT range 3. TA=-25℃~+65℃	-100		+100	mV
	VRF18_1		-75		+75	mV
	VCAMA		-3		+3	%
	VSRAM_DVFS1, VSIM1, VSIM2, AVDD28_AUD, VAUXA28, VCAMD		-1		+1	%
	VRTC		2			V
	DVDD18_DIG		-10		10	%
	Others		-5		+5	%
	ALDO and DLDO low power mode	1. Iout =0~0.05*Imax 2. VBAT range	-5		+5	%
Temperature coefficient	ALDO and DLDO	TA=-25℃~+65℃	-100		+100	ppm/C
Load transient response	VMCH, VEMC33	1. Iout=0.1mA to 50mA (slew rate=50mA/us) 2. VBAT range 3. TA=-25℃~+65℃	-5		+5	%
	VCAMA	1. Iout=1mA to Imax (slew rate=15mA/us) 2. VBAT range 3. TA=-25℃~+65℃	-3		+3	%
	VRF18_1	1. Iout=100mA-> 200mA (slew rate=100mA/us) 2. VBAT range 3. TA=-25℃~+65℃	-5		+5	%
	VCN33	1. Iout=1mA-> 350mA (slew rate=70mA/us) 2. VBAT range 3. TA=-25℃~+65℃	-5		+5	%
	VSRAM_DVFS1	1. Iout=2mA to 150mA (slew rate=150mA/us) 2. VBAT range	-4		+4	%

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Parameter	Type	Conditions	Min.	Typical	Max.	Unit
		3. TA=-25℃~+65℃				
	Others	1. Iout =1mA to Imax (slew rate=15mA/us) 2. VBAT range 3. TA=-25℃~+65℃	-5		+5	%
Turn-on rise time	ALDO and DLDO	1. Iout=0mA 2. VBAT range			300	us
Turn-on overshoot	ALDO and DLDO	1. Iout=0mA 2. VBAT range			+10	%
Output noise	ALDO	1. Freq = 10Hz to 80kHz 2. Iout = 0.01*Imax/ 0.5*Imax 3. VBAT range		90		uVrms
	DLDO			500		uVrms
PSRR	ALDO	1. 100Hz < freq < 3kHz 2. Iout = 0.01*Imax / 0.5*Imax 3. VBAT range		65		dB
	DLDO	1. Freq = 217Hz 2. Iout = 0.01*Imax / 0.5*Imax 3. VBAT range		40		dB
Short current	ALDO and DLDO	VBAT range	Imax*1.2		Imax*5	
Normal mode quiescent current	VCAMA				300	uA
	VMCH/ VEMC33/ VRF18_1				100	uA
	VSRAM_DVFS1/VCN33				200	uA
	DVDD18_DIG				5	uA
	Others				55	uA
Low power mode quiescent current	VMCH				15	uA
	ALDO and DLDO				10	uA

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2.7 Sink LDO

Table 2-7. Sink LDO specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
VBIASN sink current			200		mA
Line/Load regulation	1. VBAT range 2. TA=-25℃~+65℃ 3. Sink Imax	-150		+150	mV
Turn-on rise time	1. VBAT range 2. TA=-25℃~+65℃ 3. Iout=0 mA			300	us

2.8 Driver

Table 2-8. Driver specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
ISINK					
ISINK LED sink current	ISINK_SEL = 000		4		mA
	ISINK_SEL = 001		8		mA
	ISINK_SEL = 010		12		mA
	ISINK_SEL = 011		16		mA
	ISINK_SEL = 100		20		mA
	ISINK_SEL = 101		24		mA
ISINK dropout voltage	4 ~ 24mA VISINK drop		150	250	mV
ISINK rise/fall time	VISINK > 0.3V			3.33	uS
VIBR					
Output voltage	VIBR_SEL = 000	1.1	1.2	1.3	V
	VIBR_SEL = 001	1.2	1.3	1.4	V
	VIBR_SEL = 010	1.4	1.5	1.6	V
	VIBR_SEL = 011	1.7	1.8	1.9	V
	VIBR_SEL = 100	2.35	2.5	2.65	V
	VIBR_SEL = 101	2.65	2.8	2.95	V
	VIBR_SEL = 110	2.85	3.0	3.15	V
	VIBR_SEL = 111	3.1	3.3	3.5	V
Output current			150		mA

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2.9 Class AB/D Audio Amplifier

Table 2-9. Class AB/D audio amplifier specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Class AB Audio Amplifier					
RMS power	8Ω load, VBAT = 4.2V THD + N = 1%		850		mW
	8Ω load, VBAT = 3.7V THD + N = 1%		700		mW
	8Ω load, VBAT = 3.4V THD + N = 1%		600		mW
THD+N	1kHz, Po = 0.5Wrms, 4.2V		0.05	0.2	%
ISINK rise/fall time	VISINK > 0.3V			3.33	uS
PSRR	217Hz, Vin = 200mVpk-pk Input AC to ground	65	75		dB
	1kHz, Vin = 200mVpk-pk Input AC to ground	65	75		dB
	4kHz, Vin = 200mVpk-pk Input AC to ground	65	75		dB
	20kHz, Vin = 200mVpk-pk Input AC to ground		50		dB
Noise level	VBAT = 3.3V 0dB gain 8Ω, A-weighted			100	µV
	VBAT = 4.2V 0dB gain 8Ω, A-weighted			100	uV
Gain adjustment		6		15	dB
Gain adjustment steps			1		dB
Quiescent current	No load		3	6	mA
CMRR	VBAT = 3.4/3.8/4.2V F = 1kHz, Vin = 200mVpk-pk	49	60		dB
Class D Audio Amplifier					
RMS power	8Ω load, VBAT = 4.2V THD + N = 1%		850		mW
	8Ω load, VBAT = 3.7V THD + N = 1%		700		mW
	8Ω load, VBAT = 3.4V THD + N = 1%		600		mW
THD+N	1kHz, Po = 0.5Wrms, 4.2V			0.2	%
PSRR	217Hz, Vin = 200mVpk-pk Input AC to ground	65	75		dB
	1kHz, Vin = 200mVpk-pk Input AC to ground	65	75		dB
	4kHz, Vin = 200mVpk-pk Input AC to ground	65	75		dB
	20kHz, Vin = 200mVpk-pk Input AC to ground		50		dB
Noise level	VBAT = 3.3V 0dB gain 8Ω, A-weighted			100	µV
	VBAT = 4.2V 0dB gain			100	uV

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Parameter	Conditions	Min.	Typical	Max.	Unit
	8Ω, A-weighted				
Efficiency	VBAT = 4.2V 0.8W, 8Ω with 68uH, 1kHz	80	90		%
Gain adjustment		6		15	dB
Gain adjustment steps			1		dB
Quiescent current	No load		4	6	mA
CMRR	VBAT = 3.4/3.8/4.2V F = 1kHz, Vin = 200mVpk-pk	49	60		dB

2.10 Battery Charger

Table 2-10. Charger specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
CHRIN operating voltage		4.3	5	10.5	V
OTG B-Valid detection		0.8	2.4	4	V
VCDT CHRIN detection threshold	VCDT_VTHL[3:0] = 0000 ~ 1111	4.3		10.5	V
HV adaptive current @ pre_charge	CHRIN switch threshold (300mA => 70mA)		7		V
	CHRIN switch threshold (70mA => 300mA)		6		V
VBAT CC voltage accuracy	Programmable: 3.3~3.45, 50mV steps	-50		+50	mV
VBAT CV voltage accuracy	Programmable: 3.5~4.4 V	-30		+30	mV
VBAT OV voltage accuracy	Programmable: 3.9~4.5 V	-30		+30	mV
CC mode charging current accuracy	Programmable: 70~2000 mA (Rsense=56mohm)	TBD		TBD	mA

2.11 BC1.x

Table 2-11. BC1.x specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
BC11 charging port detection (Pre-CC current)	Standard down-stream port	35	70	94	mA
	Standard charging down-stream port	35	70	94	mA
	DP, DM short	210	300	390	mA
BC11 characteristics	DP, DM floating	210	300	390	mA
	IPU_DP, IPU_DM		9.6		uA
	IPD_DP, IPD_DM		96		uA
	VSRC on DP, DM		630		mV
	Current pulse value under 2.2V		70		mA
	Current pulse period under 2.2V		550		ms
	OSC1M, timer		5		min

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2.12 Down Load Without Battery

Table 2-12. Down Load without Battery specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
USBDL	Duration		32.0		s
	Current		450		mA

2.13 AUXADC

Table 2-13. AUXADC specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Supply voltage		-	2.8	-	V
Resolution	AUXADC_VIN	-	-	16	Bits
	Others	-	-	15	Bits
Analog-input bandwidth			0.5K		Hz
Sample rate			1K		Hz
Offset error	Relative to full-scale	-1	-	+1	%
Gain error	Relative to full-scale	-1	-	+1	%
INL	15-bit output		2		LSB
DNL	15-bit output		2		LSB

2.14 Fuel Gauge

Table 2-14. Fuel Gauge specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
FG current characteristics	Output resolution		15		Bit
	Conversion time		1/16		s
	Over-sampling ratio	2^11		2^18	
ADC characteristics	Input voltage range	-60		60	mV
	Supply		2.8		V
	Current		40		uA
	Gain error	-2		2	%
	Accuracy		0.03		%

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3 Functional Descriptions

3.1 General Descriptions

MT6325 is a fully integrated PMIC target for smart phone power provider. Figure 3-1. Is the block diagram of MT6325 PMIC.

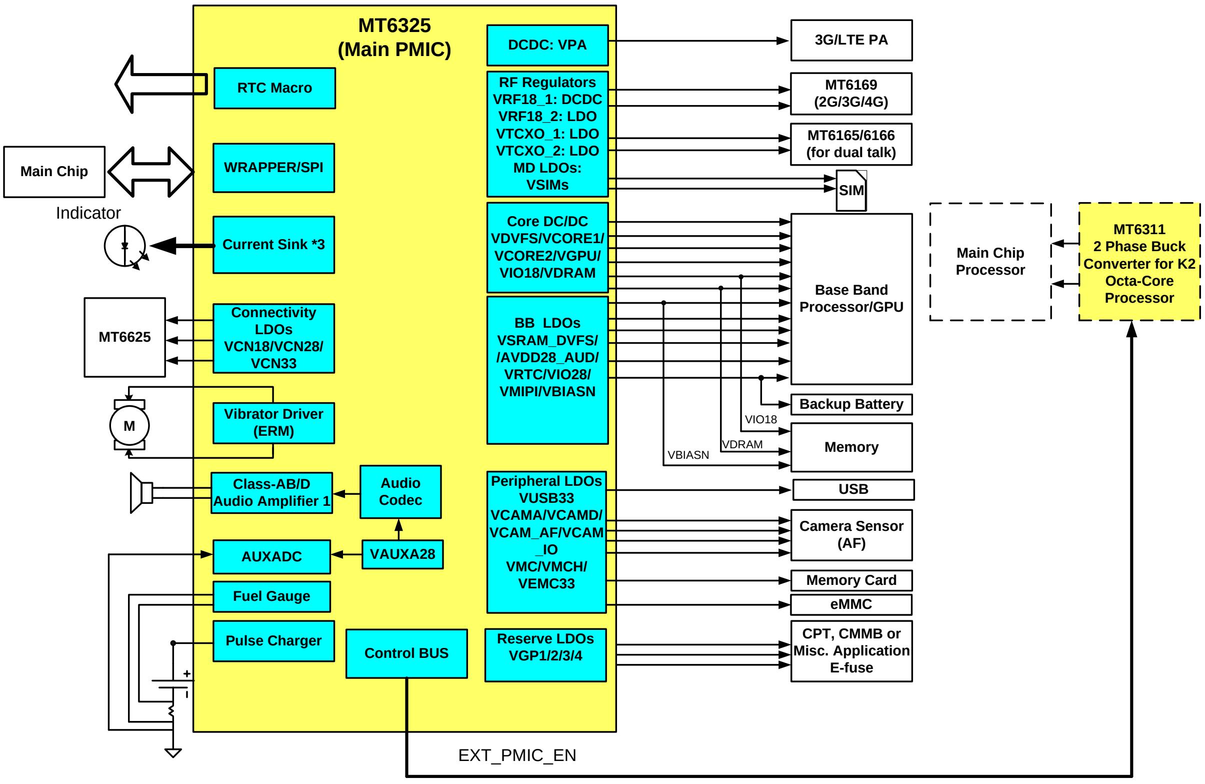

Figure 3-1. MT6325 block diagram

3.2 PMIC Functional Blocks

MT6325 manages the power supply of baseband processor, SIM cards, camera, vibrator, etc. MT6325 includes the following analog functions for use on smart phone platforms.

- LDO and BUCK: Provides regulated lower output voltage level from Li-Ion battery
- Current sink (ISINK) driver: Sink current for indicator
- Vibrator driver: Provides regulated power for vibrator with brake function.
- AUXADC: 15 bits of analog to digital converter for thermal/accessory detection monitor and measurement
- Controller: Generates power-on/off sequence, system reset and exceptional handling function

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- Charger controller: Controls/Protects battery charging procedure
- Full-set high-quality audio feature: Supports uplink/downlink audio CODEC
- Fuel gauge: Supports accurate battery capacity monitor

More detailed descriptions of each sub-block are explained in the following sections.

3.2.1 Power-On/Off Sequence

PMIC handles the power-on and power-off of the handset. If the battery voltage is neither in the UVLO state (VBAT ≥ UVLO_VTHH) nor in the thermal condition, there are 3 methods to power on the handset system.

1) Pulling PWRKEY low (User presses PWRKEY.)
2) Setting BBWAKEUP to high
3) Valid charger plug-in

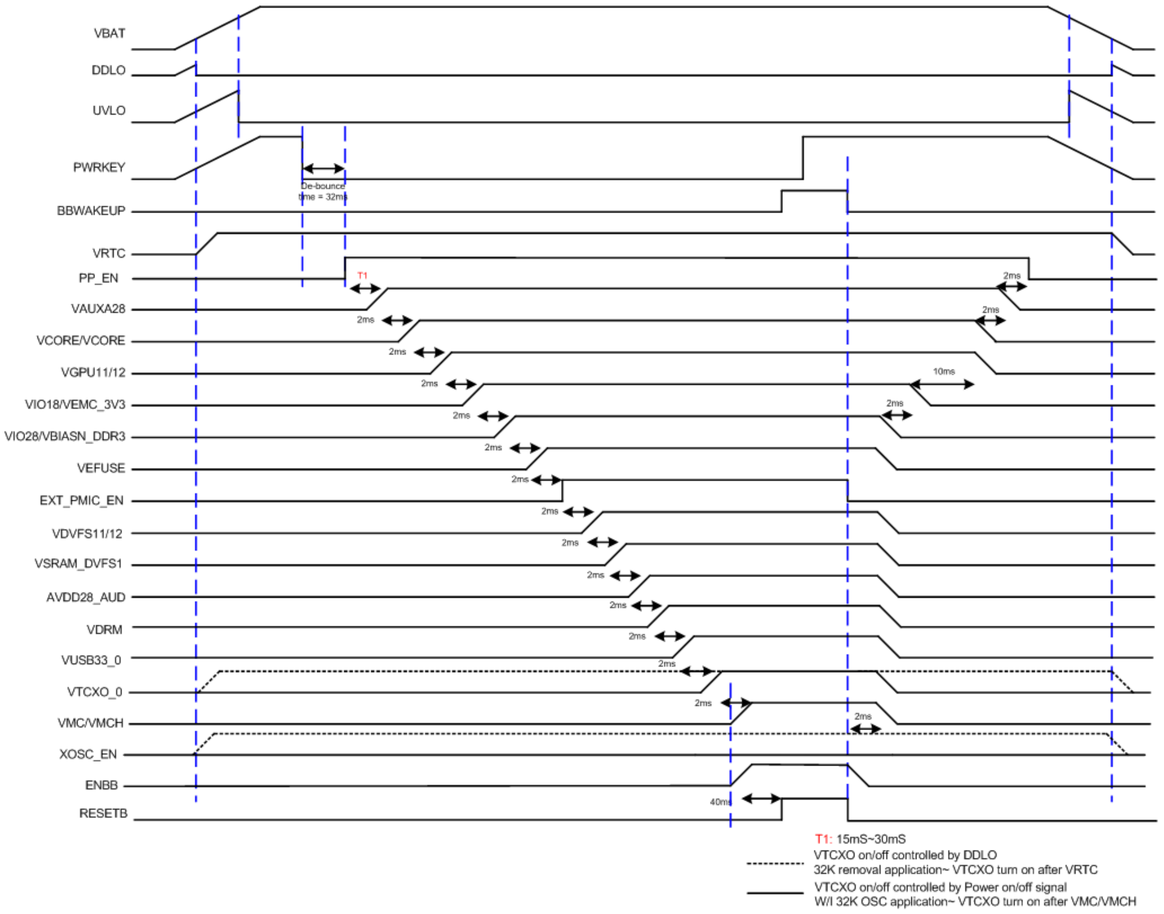

Figure 3-2. Power-on/off control sequence with XTAL by pressing PWRKEY

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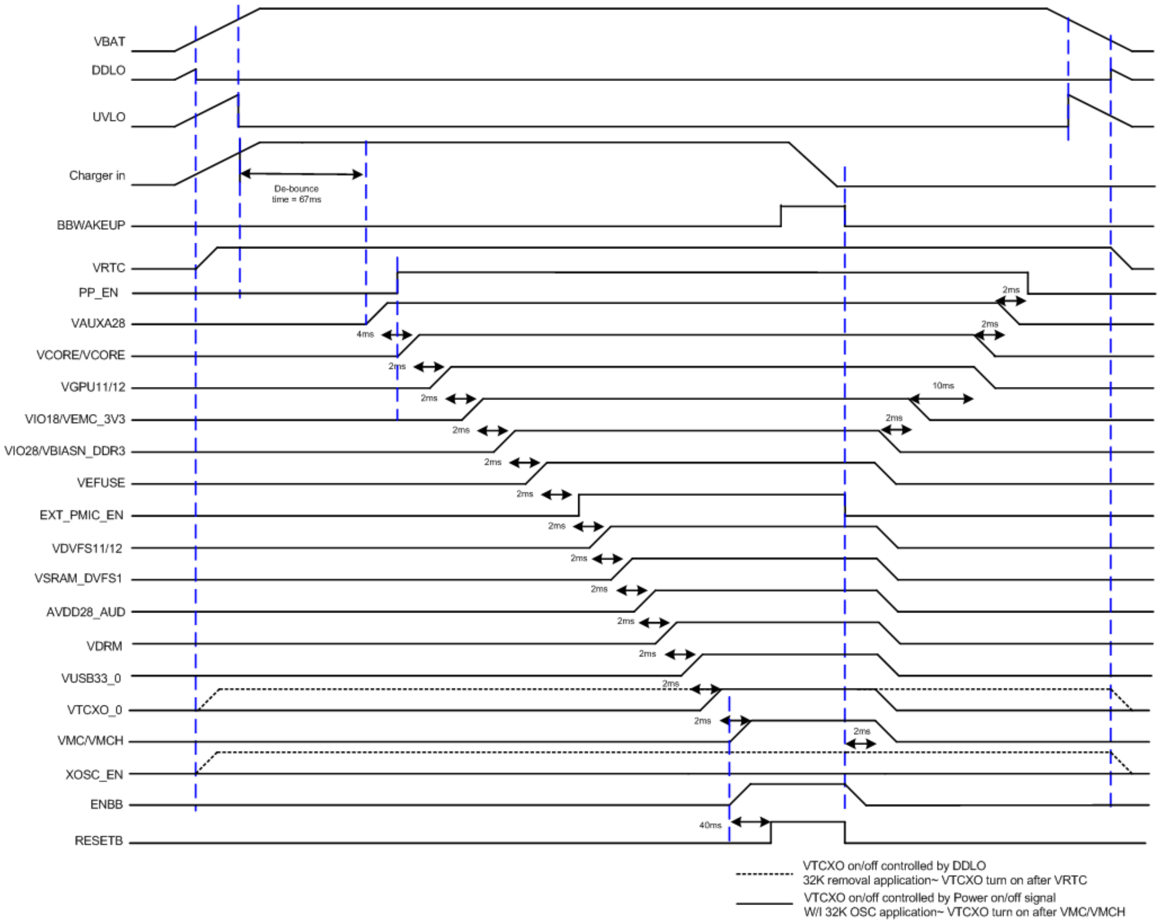

Figure 3-3. Power-on/off control sequence with XTAL by charger plug in

1. Pushing PWRKEY (pulling the PWRKEY pin to low level)
   Pulling PWRKEY low is a typical method to turn on the handset. The system reset ends at the moment when all default-on regulators are sequentially turned on. After that, the baseband will send the BBWAKEUP signal back to PMIC for acknowledgement. To successfully power on the handset, PWRKEY should be kept low until PMIC receives BBWAKEUP from the baseband.

2. RTC module generates BBWAKEUP to wake up the system.
   If the RTC module is scheduled to wake up the handset at some time, the BBWAKEUP signal will be directly sent to PMIC. In this case, BBWAKEUP becomes high at specific moment and allows PMIC power-on. This is called the RTC alarm.

3. Valid charger plug-in (CHRIN voltage within valid range)
   The charger plug-in will also turn on the handset if the charger is valid. When PMU_CHGIN input voltage> CHGIN_VTHH and VSYS>UVLO, the handset will also be powered on.

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Under-voltage lockout (UVLO)

The UVLO state in PMIC prevents start-up if the initial voltage of the main battery is below UVLO_VTH. The judgment is done by VSYSNS (with charger plugged in) and VBATSNS+VSYSNS (without charger plugged in). It ensures that the handset is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state and PMIC will be turned off by itself, except for VRTC LDO, to prevent further discharging. Once PMIC enters the UVLO state, it will draw low quiescent current. RTC LDO will still be working until DDLO disables it.

Deep discharge lockout (DDLO)

PMIC will enter the deep discharge lockout (DDLO) state when the battery voltage drops below DDLO_VTHL. In this state, VRTC LDO will be shut down. Otherwise, it will draw very low quiescent current to prevent further discharging or even damage to the cells.

Reset

PMIC contains a reset control circuit which takes effect at both power-up and power-down. The RESETB pin is held low in the beginning of power-up and returns to high after the pre-determined delay time. The delay time is controlled by a large counter, which uses the clock from the internal ring-oscillator. At power-off, the RESETB pin will return to low immediately without any delay.

Over-temperature protection

If the die temperature of PMIC exceeds 150°C, PMIC will automatically disable all regulators except for VRTC. Once the over-temperature state is resolved, a new power-on sequence will be required to enable the regulators.

3.2.2 Buck Converter and Application Reference

There are 8 buck converters in MT6325 to efficiently generate regulated power for graphic processor, digital core and circuits. The block diagram is shown in Figure 3-1. The buck converters operate with 3MHz fixed frequency pulse width modulation (PWM) mode at moderate to heavy load currents. At light load currents, the converter automatically enters Pulse Frequency Modulation (PFM) mode to save power and improve light load efficiency. It also has a force-PWM mode option to allow the converter to remain in the PWM mode regardless of the load current, so that the noise spectrum of the converter can be minimized for certain highly-noise-sensitive handset applications. The buck converters also have an internal Over-Current Protection (OCP) circuit to limit the maximum high-side power FET current in over-load conditions. It has an internal soft start circuit to control the ramp-up rate of the output voltage during start-up.

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Table 3-1. Buck converter brief specifications

BUCK name	Default Voltage (V)	Vout (Volt)	Voltage step (mV)	Imax (mA)	Default on (Y/N)	Application
VDVFS11/12	1.0	0.6~1.31	6.25	6000	Y	CPU
VCORE1	1.0	0.6~1.31	6.25	2000	Y	Digital core power down domain (CORE_PDN)
VCORE2	1.0	0.6~1.31	6.25	2500	Y	Digital core always on domain (CORE_AO)
VGPU	1.0	0.6~1.31	6.25	3000	Y	GPU
VIO18	1.8	1.8	NA	2300	Y	1V8 IO
VDRAM	By Trapping	1.1/1.2/1.35/1.5	NA	2000	Y	LPDDR4/LPDDR3/LPDDR2/PCDDR3L/PCDDR3
VPA	0.5	0.5~3.4	50	800	N	3G/LTE PA
VRF18_0	1.825	1.825	NA	450	N	MT6169

3.2.3 Low Dropout Regulator (LDOs) and Application Reference

Table 3-2. LDO types and brief specifications

Type	LDO name	Input power domain	Default Voltage	Vout (Volt)	Imax (mA)	Default on (Y/N)	Application
ALDO	VTCXO0	ISENSE or VSYSSNS	2.8	2.8	40	Y	26MHz reference clock
ALDO	VTCXO1	VBAT_LDOS1	2.8	2.8	40	N	26MHz reference clock
ALDO	VAUD28	VBAT_LDOS1	2.8	2.8	40	Y	Audio
ALDO	VAUXA28	VBAT_LDOS1	2.8	2.8	40	Y	AUXADC
ALDO	VCAMA	VBAT_LDOS1	2.8	1.5/1.8/2.5/2.8	200	N	Camera module
ALDO	VCN28	VBAT_LDOS1	2.8	2.8	40	N	Connectivity 2.8V
ALDO	VRF18_1	VBAT_LDOS1	1.825	1.825	200	N	RF power
ALDO	VBIF28	VBAT_LDOS1	2.8	2.8	20	N	Battery interface

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Type	LDO name	Input power domain	Default Voltage	Vout (Volt)	Imax (mA)	Default on (Y/N)	Application
DLDO	VSIM1	VBAT_ LDOS2	1.8	1.7/1.8/1.86/ 2.76/3.0/3.1	100	N	1st SIM card
DLDO	VSIM2	VBAT_ LDOS2	1.8	1.7/1.8/1.86/ 2.76/3.0/3.1	100	N	2nd SIM card
DLDO	VCAM_AF	VBAT_ LDOS2	2.8	1.2/1.3/1.5/1.8/ 2.5/ 2.8/3.0/3.3	200	N	Camera module
DLDO	VGP1	VBAT_ LDOS2	2.8	1.2/1.3/1.5/1.8/ 2.5/ 2.8/3.0/3.3	200	N	Cap touch
DLDO	VGP3	VBAT_ LDOS2	1.5	1.2/1.3/1.5/1.8/ 2.5/ 2.8/3.0/3.3	200	N	Sub camera module
DLDO	VMC	VBAT_ LDOS2	3.3	1.8/3.3	200	Y	SD 2.0/3.0 memory card
DLDO	VMCH	VBAT_ LDOS3	3.3	3/3.3	800	Y	SD 3.0 memory card
DLDO	VEMC33	VBAT_ LDOS4	3.3	3/3.3	400	Y	eMMC 3.3V
DLDO	VIO28	VBAT_ LDOS4	2.8	2.8	200	Y	2V8 IO
DLDO	VCN33	VBAT_ LDOS4	3.3	3.3/3.4/3.5/3.6	350	N	Connectivity 3.3V
DLDO	VUSB33	VBAT_ LDOS4	3.3	3.3	50	Y	USB 3.3V
DLDO	VEFUSE	VBAT_ LDOS5	1.8	1.6/1.7/1.8/1.9/ 2.0	200	Y	Main chip Efuse power
DLDO	VCAM_IO	VBAT_ LDOS5	1.8	1.2/1.3/1.5/1.8	200	N	Camera module
DLDO	VCN18	VBAT_ LDOS5	1.8	1.8	150	N	Connectivity 1.8V
DLDO	VMIPI	VBAT_ LDOS5	1.8	1.2/1.3/1.5/1.8	150	N	MIPI interface
DLDO	VCAMD	AVDD18_ SLDO2	1.3	0.9/1.0/1.1/1.22/ 1.3/1.5	500	N	Camera module
DLDO	VGP2	AVDD18_ SLDO2	1.2	1.2/1.3/1.5	200	N	MHL

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Type	LDO name	Input power domain	Default Voltage	Vout (Volt)	Imax (mA)	Default on (Y/N)	Application
Sink LDO	VBIASN	AVDD18_SLDO1	0.2	0.2~0.8	200	Y	DRAM driving
DLDO	VSRAM_DVFS1	AVDD18_SLDO1	1.0125	0.6~1.31	400	Y	CPU SRAM
VRTC	VRTC	ISENSE or VSYSSNS	2.8	2.8	2	Y	Real-time clock
DVDD18_DIG	DVDD18_DIG	ISENSE or VSYSSNS	1.8	1.8	20	Y	Internal digital

3.2.4 Drivers

MT6325 supports 3 indicator LED drivers at most. The following figure depicts the major application for indicator LEDs drivers.

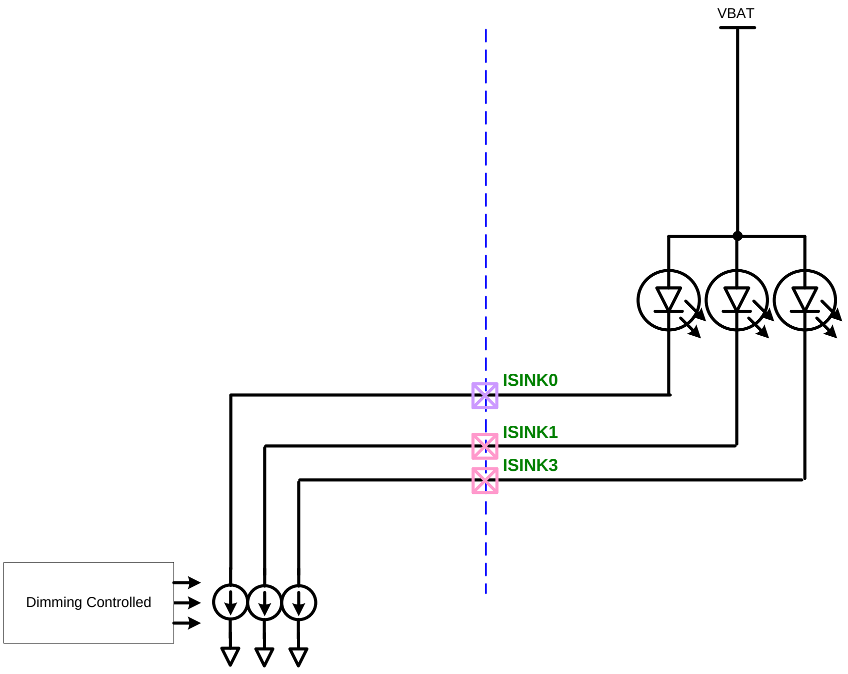

Figure 3-4. Configuration for indicator LED drivers

3.2.5 Vibrator Driver

The VIBR driver power allows up to 150mA current for is for ERM (Eccentric Rotating Mass) vibrator with programmable output voltage. The following figure depicts the major application for ERM driver.

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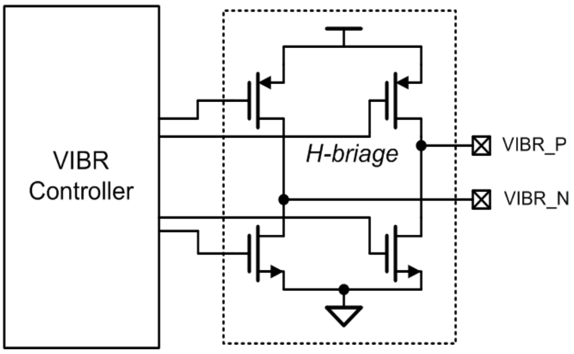

Figure 3-5. Configuration for ERM driver

3.2.6 Audio CODEC and Accessory Detection

3.2.6.1 Block Descriptions

The block diagram of audio codec is illustrated below. The audio uplink path is composed of PGA and audio ADC. There are three input pairs of the uplink path to support dual-MIC, earphone-MIC, voice wakeup and digital MIC. The audio downlink is composed of stereo audio DACs, stereo headphone drivers and a mono voice driver. High-fidelity audio is reproduced on headphones and clear mobile speech on earpiece is driven by voice drivers. The internal high output power loud-speaker amplifier is also embedded. The necessary MIC bias voltages and multi-key accessory detection are also provided by this completed audio codec.

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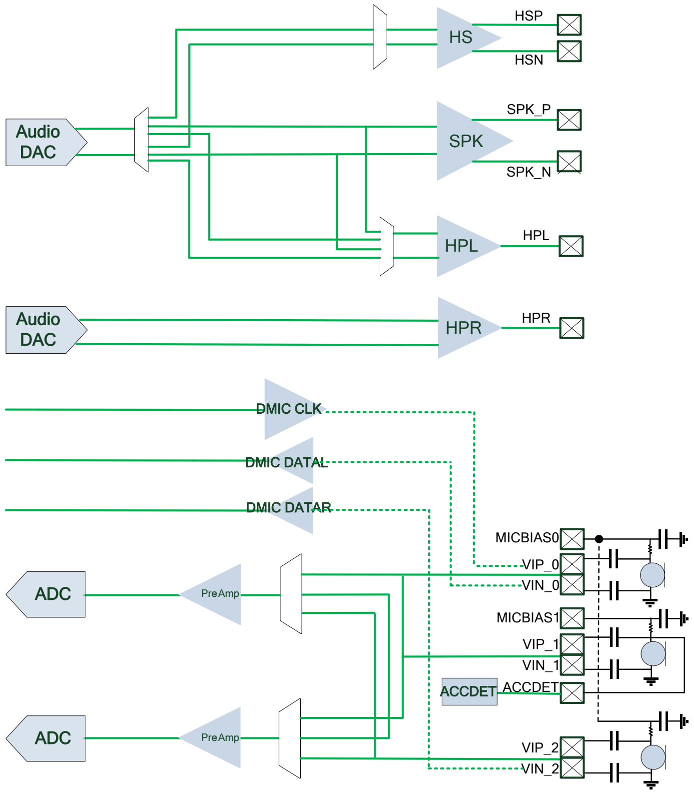

Figure 3-6. Audio CODEC and accessory detection block diagram

3.2.6.2 Functional Specifications

Symbol	Parameter	Min.	Typical	Max.	Unit
T	Operating temperature	-25		85	°C
VMIC	Microphone biasing voltage	1.7		2.5	V
IMIC	Current draw from microphone bias			3	mA
Uplink path					
Analog MIC path					
IDC	Current consumption for single channel		1.5		mA
SNDR	Signal to noise and distortion ratio Input Level: -60 dbmo Input Level: 0 dbmo		 25 80		 dB dB
RIN	Input impedance (differential)	13	20	27	KΩ
ICN	Idle channel noise			-67	dBmo
xTalk	Crosstalk level			-66	dBmo
Digital MIC path					
DCLK	DMIC clock frequency		3.25/1.62/ 0.8125/ 0.513		MHz
DTY	DMIC clock duty cycle	40		60	%
DCRT	DMIC clock rise time (MaxCL = 65p)			10	ns
DCFT	DMIC clock fall time (MaxCL = 65p)			10	ns
ICDD	Input capacitance for DMIC data			45	pF

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Voice downlink specification

Symbol	Parameter	Min.	Typical	Max.	Unit
T	Operating temperature	-25		85	°C
AVDD18	1.8V analog power supply	1.7	1.8	1.9	V
IDC	Quiescent current consumption		6		mA
VOUT	Full-scale output signal level		1	1.7	Vrms
RLOAD	Output resistor load	16	32		Ω
CLOAD	Output capacitor load			500	pF
SNR	Signal to noise ratio		100		dB
ICN	Idle channel noise of transmit path			-67	dBm0

Audio downlink specification

Symbol	Parameter	Min.	Typical	Max.	Unit
T	Operating temperature	-25		85	°C
AVDD18	1.8V analog power supply	1.7	1.8	1.9	V
IDC	Quiescent current consumption		6		mA
BW	Signal bandwidth	20		20,000	Hz
VOUT	Full-scale output signal level		0.5	1	Vrms
RLOAD	Output resistor load		32		Ω
CLOAD	Output capacitor load			250	pF
SNR	Signal to noise ratio (A-weighted)		100		dBA
THD	Total harmonic distortion		-85		dBc
xTalk	Channel separation (Crosstalk)		80		dB
T	Operating temperature	-25		85	°C

3.2.7 Class-AB/D Audio Amplifier

MT6325 has one built-in channel high efficiency class AB/D audio power amplifier capable of delivering 0.7 watt of power on an 8 ohm BTL load from a 3.7V battery supply. Over-current protection is integrated. MT6325 also has built-in receiver mode for 2-in-1 loudspeaker which supports multi-purpose loudspeaker without any extra BOM cost. The output power can reach 97mW onto 8 ohm speaker load. The block diagram is shown below.

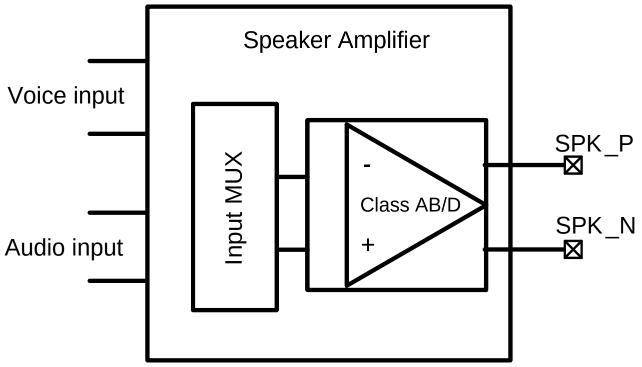

Figure 3-7. Block diagram of class-AB/D

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3.2.8 Battery Charger (Charger Controller)

The charger controller senses the charger input voltage from either a standard AC-DC adaptor or an USB charger. When the charger input voltage is within a pre-determined range, the charging process will be activated. This detector resists higher input voltages than other parts of PMIC.

3.2.8.1 Block Descriptions

The block diagram of battery charger is illustrated below.

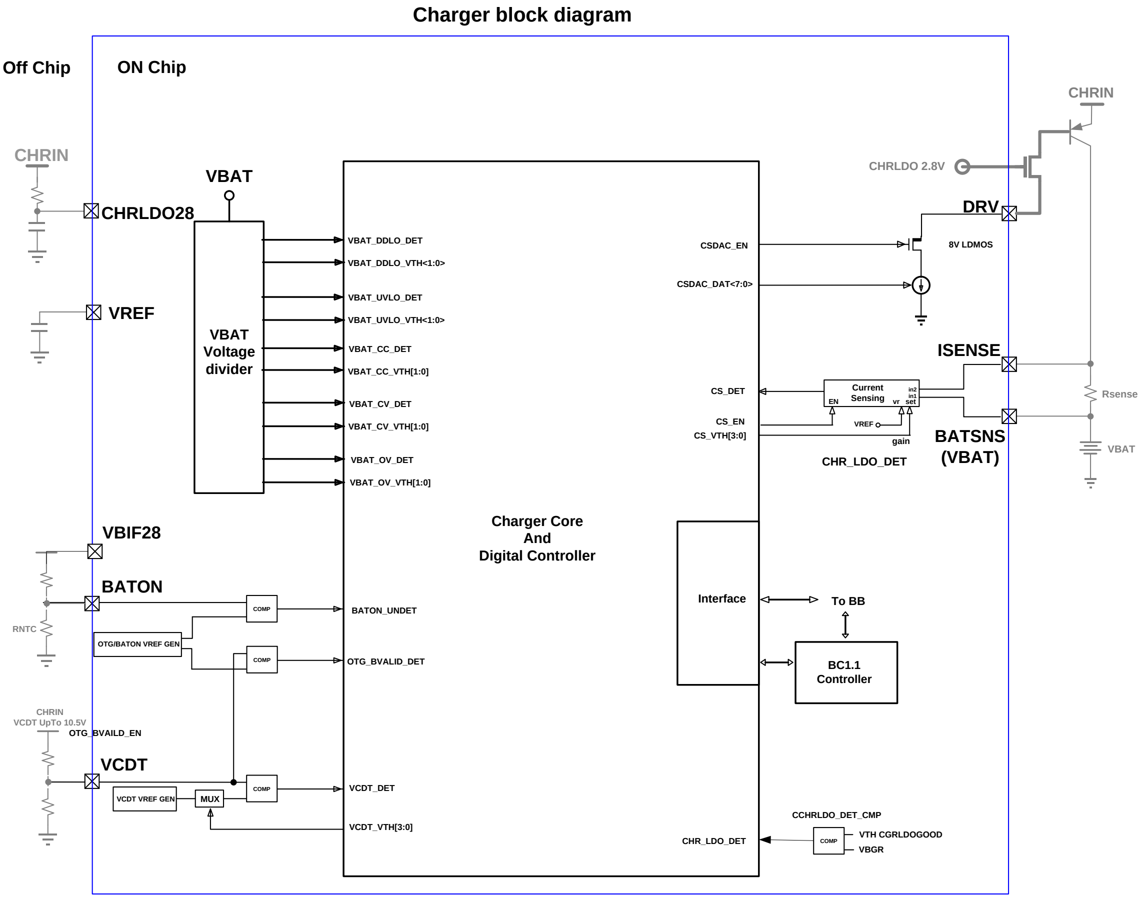

Figure 3-8. Block diagram of battery charger

3.2.8.1.1 Charger Detection

Whenever an invalid charging source is detected (> 7.0V, software default setting), the charger detector will stop the charging process immediately to avoid burning out the chip or even the phone. Furthermore, if the charger-in level is not high enough (< 4.3V), the charger will also be disabled to avoid improper charging behavior.

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3.2.8.1.2 Charging Control

When the charger is active, the charger controller will manage the charging phase according to the battery status. During the charging period, the battery voltage is constantly monitored. The battery charger supports pre-charge mode (VBAT < 3.0V, PMIC power-off state), CC mode (Constant Current mode or fast charging mode at the range of 3.0V < VBAT < 4.2V, CV default voltage) and CV mode (Constant Voltage mode) to optimize the charging procedure for Li-ion battery. See the figure below for the charging states diagram.

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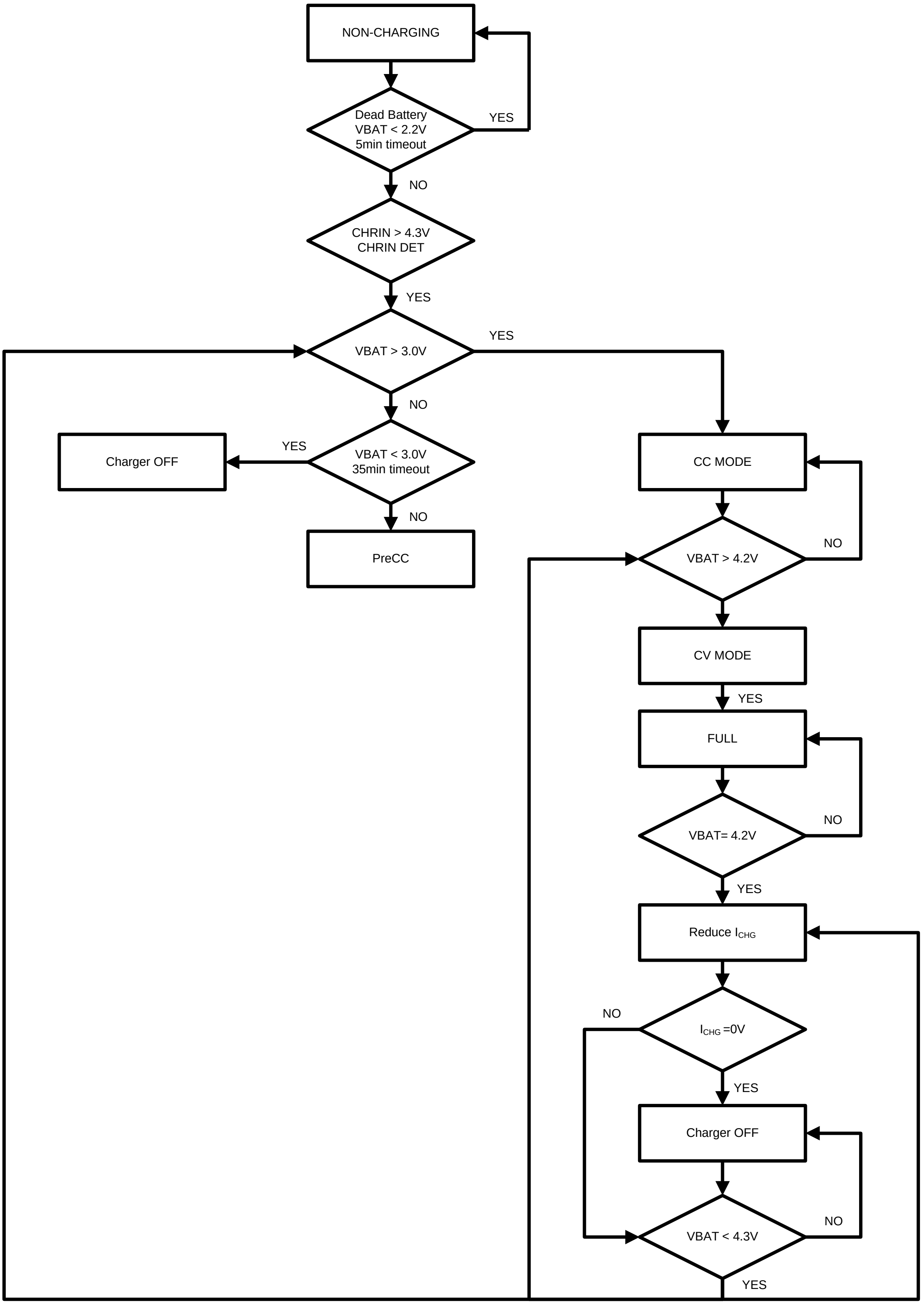

Figure 3-9. The flow chart of charging states

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Pre-charge mode

When the battery voltage is in the UVLO state, the charger will operate in the pre-charge mode. There are two steps in this mode. While the battery voltage is deeply discharged below 2.2V, IUNIT trickle charging current is applied to the battery.

The IUNIT trickle charging current is about 550ms pulse 70mA current when VBAT is under 2.2V.

When the battery voltage exceeds 2.2V, i.e. the PRECC1 stage, the closed-loop pre-charge will be enabled. The voltage drop across the external RSENSE is kept around 16.8mV (AC charger) or 3.92mV (USB host). The closed-loop pre-charge current can be calculated:

$$I_{PRECC1,\,AC\ adapter} = \frac{V_{SENSE}}{Rsense} = \frac{16.8mV}{Rsense}$$

$$I_{PRECC1,USBHOST} = \frac{V_{SENSE}}{Rsense} = \frac{3.92mV}{Rsense}$$

Constant current mode

As the battery is charged up and over 3.0V, it can switch to the CC mode. (CHR_EN should be high) In the CC mode, several charging currents can be set by programming registers or the external RSENSE resistor. The charging current can be determined by CS_VTH/RSENSE, where CS_VTH is programmed by registers. For example, if RSENSE is selected as 0.056ohm, the CC mode charging current can be set from 70 to 2,000mA. It can accommodate the battery charger to various charger inputs with different current capabilities.

Constant-voltage mode and over-voltage protection (OV)

When the battery voltage reaches about 4.2V, a constant voltage is used for charging. This is called the full-voltage charging mode or constant-voltage charging mode in correspondence to a linear charger. When the battery voltage actually reaches 4.2V, the charging current gradually decreased step-by-step, and the end-of-charging process starts. It may prolong the charging and detecting period for acquiring optimized full charging volume. The charging process is completed once the current reaches termination current automatically and this mechanism is optimized for different battery packs. Whenever the battery voltage exceeds 4.3V (programmed by SW), a hardware OV protection will be activated and turns off the charger immediately.

3.2.8.1.3 BC1.x Dead-Battery Support

MT6325 also supports dead-battery condition BC1.x. These specifications protect dead-battery charging by timer and trickle current. Once the battery voltage is below 2.2V, a period (TUNIT) of trickle current (IUNIT) will be applied to the battery.

If the battery voltage is still below 2.2V after the trickle current is applied, the charger will be disabled. On the other hand, once the battery voltage rises to above 2.2V, the charger will enter the PRECC1 stage, and the charging current will be 70mA or 300mA depending on the type of the charging port.

When the battery is below 3.0V, the charger will charge the battery by the PRECC1 current.

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A dedicated 5 min. (T1) timer will be timed out and disable the charger if the battery voltage is always below 2.4V under charging. Another 35 min. (T2) timer will also be timed out and disable the charger if the battery voltage is always kept between 2.7V and 3.0V under charging.

The trickle current (IUNIT) and two dedicated timers protect the charging action if the battery is dead.

3.2.8.1.4 Auto Power-On Mode (USB down load without battery)

MT6325 features a default auto power-on mode (or USB DL without battery) no matter with or without battery. Users can disable auto power-on by adding external pull-high resistor on the FCHR_ENB pin. They can still initiate USB DL (auto power-on) by pressing DL_KEY or under valid BAT_ON information (decided by customers' PCB options). Nonetheless, DL_KEY supports key function in normal mode. The valid BAT_ON information can be detected through battery's NTC when it is connected to pin BAT_ON of MT6325.

3.2.9 AUXADC

3.2.9.1 Block Descriptions

The auxiliary ADC includes the following functional blocks:

1. Analog multiplexer: Selects signal from one of the input channels. Real-world messages to be monitored, e.g. temperature, should be transferred to the voltage domain.
2. 15-bit A/D converter: Converts the multiplexed input signal to 15-bit digital data.

Table 3-3. Application and input range of ADC channels

Channel	Application	Input range [V]
0	BATSNS	2.5 ~ 4.5
1	ISENSE	2.5 ~ 4.5
2	VCDT	0 ~ 1.8
3	BATON	0.1 ~ 2.7
5	ACCDET	0 ~ 1.8
7	AUXADC_VIN	0 ~ 1.8
others	Internal use	N/A

3.2.10 Fuel Gauge

The fuel gauging system includes a dedicated ADC for Li-Ion battery current measurement and utilizes the measurement ADC (AUXADC) for battery voltage and temperature measurement. The battery state-of-charge (SOC) estimation is performed by the software using the three measuring methods and the accumulated current measurement. The application diagram of the fuel gauging system is shown in the figure below, where an external resistor is used to convert the current drawn from the battery into a voltage which is then measured by FG ADC. The value of the external resistor must be chosen so that the maximum current during charging or discharging will not cause ADC to exceed its input voltage range.

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The principle of operation of the fuel gauge relies on a combination of Coulomb counting and light load battery voltage measurement. Coulomb counting provides an estimate of the charge that has been withdrawn or delivered to the battery, while battery voltage measurement proves a good estimate of the battery SOC under low-load conditions. The battery voltage measurement compensates for error accumulation during the current integration inherent in Coulomb counting. The hardware also includes necessary modes to allow for simultaneous current and voltage measurement which can be utilized to estimate the battery impedance.

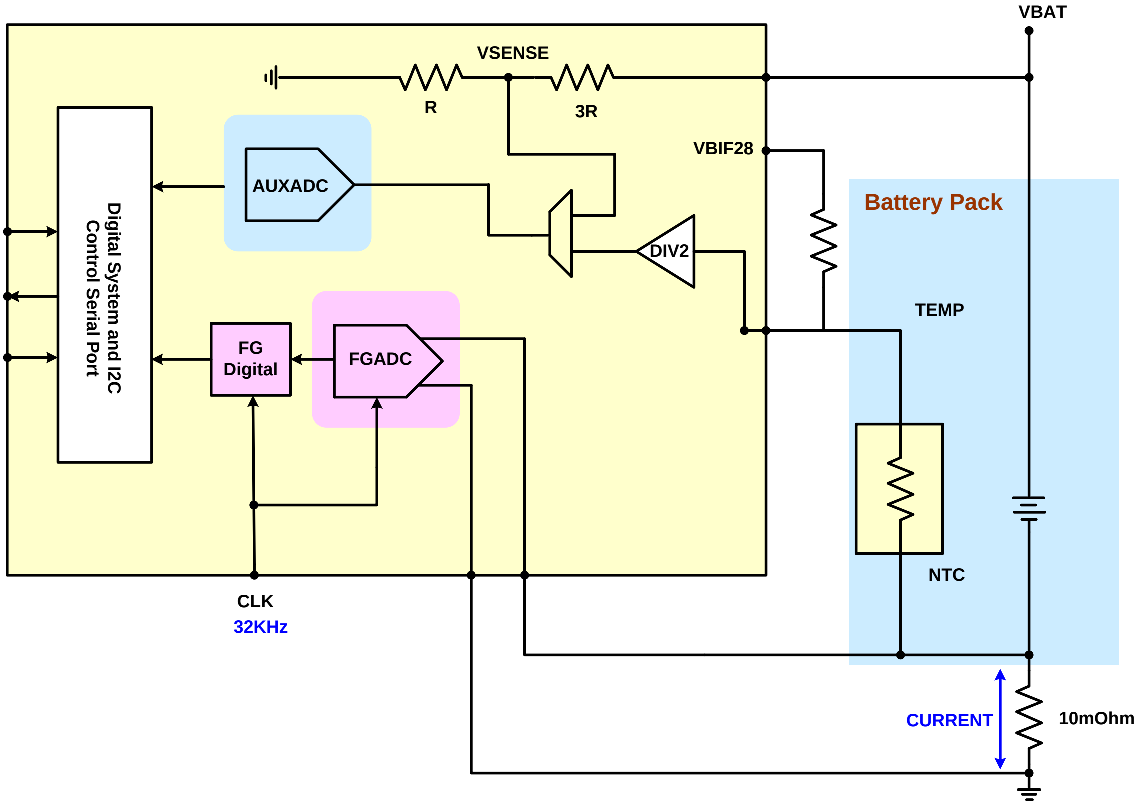

Figure 3-10. Fuel gauge block diagram and external connection

3.2.11 Real-time Clock

The Real Time Clock (RTC) module provides time and data information. The clock is based on a 32.768kHz oscillator with an independent power supply. When the mobile handset is powered off, a dedicated regulator supplies the RTC block. If the main battery is not present, a backup supply such as a small mercury cell battery or a large capacitor will be used. In addition to providing timing data, an alarm interrupt is generated and can be used to power up the baseband core via the BBWAKEUP pin. Regulator interrupts corresponding to seconds, minutes, hours and days can be generated whenever the time counter value reaches a maximum value (e.g. 59 for seconds and minutes, 23 for hours, etc.). The year span is supported up to 2,127. The maximum day-of-month values, which depend on the leap year condition, are stored in the RTC block.

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In MT6325, RTC module also supports function without 32kHz crystal. It can be configured by hardware option. The two configurations are shown below. While crystal is absent, RTC module has an embedded 32kHz oscillator to assist life time extension after master 32kHz clock is off.

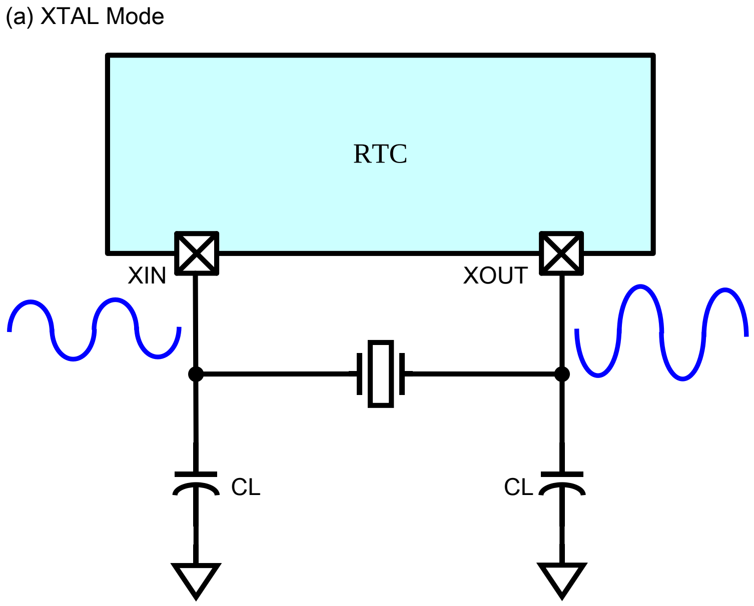

Figure 3-11. RTC configuration methods for XTAL

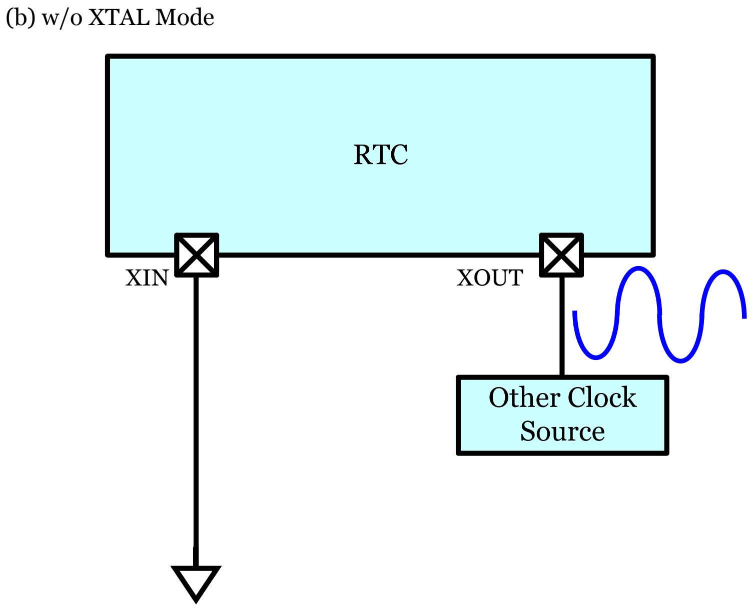

Figure 3-12. RTC configuration methods for w/o XTAL mode

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3.2.11.1 32kHz Crystal Oscillator (XOSC32)

The low-power 32kHz crystal oscillator XOSC32 is designed to work with an external piezoelectric 32.768kHz crystal and a load composed of two functional capacitors. The key performance is shown in the table below.

Table 3-4. Functional specifications of XOSC32

Symbol	Parameter	Min.	Typical	Max.	Unit
VRTC	RTC module power	1.1	2.8	3.0	V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle	20		80	%
I	Current consumption		5		µA
T	Operating temperature	-20		80	℃

The minimum VRTC value means if the crystal oscillator starts up successfully, then the minimum VRTC for the clock to still be alive is 1.1V.

Since the crystal parameters determine the oscillation allowance, below are a few recommendations for the crystal parameters to be used well with XOSC32 in MT6325.

Table 3-5. Recommended parameters of 32kHz crystal

Symbol	Parameter	Min.	Typical	Max.	Unit
F	Frequency range		32768		Hz
GL	Drive level	0.5			uW
Δf/f	Frequency tolerance		+/- 20		ppm
ESR	Series resistance		50	70	KΩ
Co	Static capacitance		0.9	2	pF
CL[1]	Load capacitance	6		12.5	pF

Under such CL range and crystal, the –R is greater than 3 times. If CL is selected larger, the frequency accuracy will be decreased, and the –R will degrade too.

3.2.12 Interrupt and Watchdog

3.2.12.1 Interrupt

Here are interrupt lists of PMIC to inform BB IC:

1. Key pressed and released interrupt

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- PWRKEY: Interrupt is issued when PWRKEY is pressed (and released, set by the register). After receiving the interrupt, the software will read the PWRKEY_DEB status to see if it is pressed or released.
- HOMEKEY: Interrupt is issued when HOMEKEY is pressed (and released, set by the register). After receiving the interrupt, the software will read the HOMEKEY_DEB status to see if it is pressed or released.

2. Thermal interrupt
   PMIC issues THR_H interrupt for the software high power latch if PMIC die temperature is over thermal regulation high threshold (e.g. 125°c) and issues THR_L for software latch release if PMIC die temperature goes from thermal regulation high threshold (e.g. 125°c) back to under thermal regulation low threshold (e.g. 110°c). The thermal regulation high/low threshold is adjustable.
3. Charger related interrupt
4. Battery voltage/current H/L interrupt
   There are two groups of VBAT detection interrupts.
   1) VBAT detected by AUXADC
      If VBAT is higher than the threshold specified by a register setting, the HIGHBATTERY interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the LOWBATTERY interrupt will be issued.
   2) VBAT detected by fuel gauge
      If VBAT is higher than the threshold specified by a register setting, the VBAT_H interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the VBAT_L interrupt will be issued.
5. Fuel-Gauge
6. Speaker OC interrupt
   PMIC supports speaker OC interrupt generation which uses PWM detection method.
7. BIF
8. VWLED
9. Buck OC interrupt
   There are 9 bucks and each has its individual interrupt which uses PWM detection method.
10. LDO OC interrupt
    PMIC supports LDO OC interrupt generation. It will be issued if any one of the LDOs has OC condition.
11. RTC interrupt
12. AUDIO interrupt
    Audio interrupt can inform AP playback of the audio status.
13. ACCDET interrupt
    This is for headphone detection.

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Table 3-6. MT6325 interrupts

Module name	Interrupt Name	ENABLE	ENABLE ADR	STATUS	STATUS ADR	Level/Edge	Default EN	De-bounce time	Status Clear Condition
STRUP	PWRKEY	RG_INT_EN_PWRKEY	0x0296 bit0	RG_INT_STATUS_PWRKEY	0x02AE bit0	edge(rising & falling)	1	50ms (in STRUP)	Write 1 Clear
STRUP	HOMEKEY	RG_INT_EN_HOMEKEY	0x0296 bit1	RG_INT_STATUS_HOMEKEY	0x02AE bit1	edge(rising & falling)	0	50ms (in STRUP)	Write 1 Clear
STRUP	PWRKEY_R	RG_INT_EN_PWRKEY_R	0x0296 bit2	RG_INT_STATUS_PWRKEY_R	0x02AE bit2	edge(rising)	1	50ms (in STRUP)	Write 1 Clear
STRUP	HOMEKEY_R	RG_INT_EN_HOMEKEY_R	0x0296 bit3	RG_INT_STATUS_HOMEKEY_R	0x02AE bit3	edge(rising)	0	50ms (in STRUP)	Write 1 Clear
AUXADC	THR_H	RG_INT_EN_THR_H	0x0296 bit4	RG_INT_STATUS_THR_H	0x02AE bit4	edge(rising)	0	50ms (in STRUP)	Write 1 Clear
AUXADC	THR_L	RG_INT_EN_THR_L	0x0296 bit5	RG_INT_STATUS_THR_L	0x02AE bit5	edge(rising)	0	50ms (in STRUP)	Write 1 Clear
AUXADC	BAT_H	RG_INT_EN_BAT_H	0x0296 bit6	RG_INT_STATUS_BAT_H	0x02AE bit6	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	BAT_L	RG_INT_EN_BAT_L	0x0296 bit7	RG_INT_STATUS_BAT_L	0x02AE bit7	level (high active)	0	V (in AUXADC)	Write 1 Clear
BIF	BIF	RG_INT_EN_BIF	0x0296 bit8	RG_INT_STATUS_BIF	0x02AE bit8	level (high active)	0	V(in BIF)	Write 1 Clear
RTC	RTC	RG_INT_EN_RTC	0x0296 bit9	RG_INT_STATUS_RTC	0x02AE bit9	level (low active)	0	No	Write 1 Clear
Audio	AUDIO	RG_INT_EN_AUDIO	0x0296 bit10	RG_INT_STATUS_AUDIO	0x02AE bit10	level (high active)	0	No	Write 1 Clear
Audio	VOW	RG_INT_EN_VOW	0x0296 bit11	RG_INT_STATUS_VOW	0x02AE bit11	level (high active)	0	No	Write 1 Clear
Accdet	ACCDET	RG_INT_EN_ACCDET	0x0296 bit12	RG_INT_STATUS_ACCDET	0x02AE bit12	level (high active)	0	No	Write 1 Clear
STRUP	NI_LBAT_INT	RG_INT_EN_NI_LBAT_INT	0x0296 bit15	RG_INT_STATUS_NI_LBAT_INT	0x02AE bit15	edge(rising)	0	150us (in STRUP)	Write 1 Clear
Regulator	VDVFS11_OC	RG_INT_EN_VDVFS11_OC	0x029C bit0	RG_INT_STATUS_VDVFS11_OC	0x02B0 bit0	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VDVFS12_OC	RG_INT_EN_VDVFS12_OC	0x029C bit1	RG_INT_STATUS_VDVFS12_OC	0x02B0 bit1	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VRF18_0_OC	RG_INT_EN_VRF18_0_OC	0x029Cbit2	RG_INT_STATUS_VRF18_0_OC	0x02B0 bit2	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VDRAM_OC	RG_INT_EN_VDRAM_OC	0x029Cbit3	RG_INT_STATUS_VDRAM_OC	0x02B0 bit3	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear

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Module name	Interrupt Name	ENABLE	ENABLE ADR	STATUS	STATUS ADR	Level/Edge	Default EN	De-bounce time	Status Clear Condition
Regulator	VGPU_OC	RG_INT_EN_VGPU_OC	0x029C bit4	RG_INT_STATUS_VGPU_OC	0x02B0 bit4	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VCORE1_OC	RG_INT_EN_VCORE1_OC	0x029C bit5	RG_INT_STATUS_VCORE1_OC	0x02B0 bit5	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VCORE2_OC	RG_INT_EN_VCORE2_OC	0x029C bit6	RG_INT_STATUS_VCORE2_OC	0x02B0 bit6	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VPA_OC	RG_INT_EN_VPA_OC	0x029C bit8	RG_INT_STATUS_VPA_OC	0x02B0 bit8	level (high active)	0	PMW deb (in STRUP)	Write 1 Clear
Regulator	VIO18_OC	RG_INT_EN_VIO18_OC	0x029C bit7	RG_INT_STATUS_VIO18_OC	0x02B0 bit7	level (high active)	1	PMW deb (in STRUP)	Write 1 Clear
LDO	LDO_OC	RG_INT_EN_LDO_OC	0x029C bit9	RG_INT_STATUS_LDO_OC	0x02B0 bit9	level (high active)	1	100/200/400/800us (in INTCTRL)	Write 1 Clear
AUXADC	BAT2_H	RG_INT_EN_BAT2_H	0x029C bit10	RG_INT_STATUS_BAT2_H	0x02B0 bit10	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	BAT2_L	RG_INT_EN_BAT2_L	0x029C bit11	RG_INT_STATUS_BAT2_L	0x02B0 bit11	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	VISMPS0_H	RG_INT_EN_VISMPS0_H	0x029C bit12	RG_INT_STATUS_VISMPS0_H	0x02B0 bit12	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	VISMPS0_L	RG_INT_EN_VISMPS0_L	0x029C bit13	RG_INT_STATUS_VISMPS0_L	0x02B0 bit13	level (high active)	0	V (in AUXADC)	Write 1 Clear
AUXADC	AUXADC_IMP	RG_INT_EN_AUXADC_IMP	0x029C bit14	RG_INT_STATUS_AUXADC_IMP	0x02B0 bit14	level (high active)	0	V (in AUXADC)	Write 1 Clear
Speaker	SPKL_D	RG_INT_EN_SPKL_D	0x02A2 bit12	RG_INT_STATUS_SPKL_D	0X02B2 bit12	level (high active)	0	V (in SPK)	Write 1 Clear
Speaker	SPKL_AB	RG_INT_EN_SPKL_AB	0x02A2 bit13	RG_INT_STATUS_SPKL_AB	0X02B2 bit13	level (high active)	0	V (in SPK)	Write 1 Clear
Charger	OV	RG_INT_EN_OV	0x02A2 bit0	RG_INT_STATUS_OV	0X02B2 bit0	edge(rising)	1	4us (in PCHR_DIG)	Write 1 Clear
Charger	BVALID_DET	RG_INT_EN_BVALID_DET	0x02A2 bit1	RG_INT_STATUS_BVALID_DET	0X02B2 bit1	level (high active)	1	0/100/200/400us (in INTCTRL)	Write 1 Clear
Charger	VBATON_UNDET	RG_INT_EN_VBATON_UNDET	0x02A2 bit2	RG_INT_STATUS_VBATON_UNDET	0X02B2 bit2	level (high active)	1	0/100/200/400us (in INTCTRL)	Write 1 Clear
Charger	WATCHDOG	RG_INT_EN_WATCHDOG	0x02A2 bit3	RG_INT_STATUS_WATCHDOG	0X02B2 bit3	level (high active)	1	N	Write 1 Clear
Charger	PCHR_CM_VDEC	RG_INT_EN_PCHR_CM_VDEC	0x02A2 bit4	RG_INT_STATUS_PCHR_CM_VDEC	0X02B2 bit4	edge(rising)	0	N	Write 1 Clear
Charger	CHRDET	RG_INT_EN_CHRDET	0x02A2 bit5	RG_INT_STATUS_CHRDET	0X02B2 bit5	edge(rising & falling)	1	50ms (in STRUP)	Write 1 Clear

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Module name	Interrupt Name	ENABLE	ENABLE ADR	STATUS	STATUS ADR	Level/Edge	Default EN	De-bounce time	Status Clear Condition
Charger	PCHR_CM_VINC	RG_INT_EN_PCHR_CM_VINC	0x02A2 bit6	RG_INT_STATUS_PCHR_CM_VINC	0X02B2 bit6	edge(rising)	0	N	Write 1 Clear
FGADC	FG_BAT_H	RG_INT_EN_FG_BAT_H	0x02A2 bit7	RG_INT_STATUS_FG_BAT_H	0X02B2 bit7	edge(rising)	0	N	Write 1 Clear
FGADC	FG_BAT_L	RG_INT_EN_FG_BAT_L	0x02A2 bit8	RG_INT_STATUS_FG_BAT_L	0X02B2 bit8	edge(rising)	0	N	Write 1 Clear
FGADC	FG_CUR_H	RG_INT_EN_FG_CUR_H	0x02A2 bit9	RG_INT_STATUS_FG_CUR_H	0X02B2 bit9	edge(rising)	0	N	Write 1 Clear
FGADC	FG_CUR_L	RG_INT_EN_FG_CUR_L	0x02A2 bit10	RG_INT_STATUS_FG_CUR_L	0X02B2 bit10	edge(rising)	0	N	Write 1 Clear
FGADC	FG_ZCV	RG_INT_EN_FG_ZCV	0x02A2 bit11	RG_INT_STATUS_FG_ZCV	0X02B2 bit11	edge(rising)	0	N	Write 1 Clear

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3.2.12.2 Watchdog Reset

WDTRSTB_IN is the watchdog reset from AP. PMIC resets all modules to initial state when receiving watchdog reset from AP.

3.2.13 SPI Interface

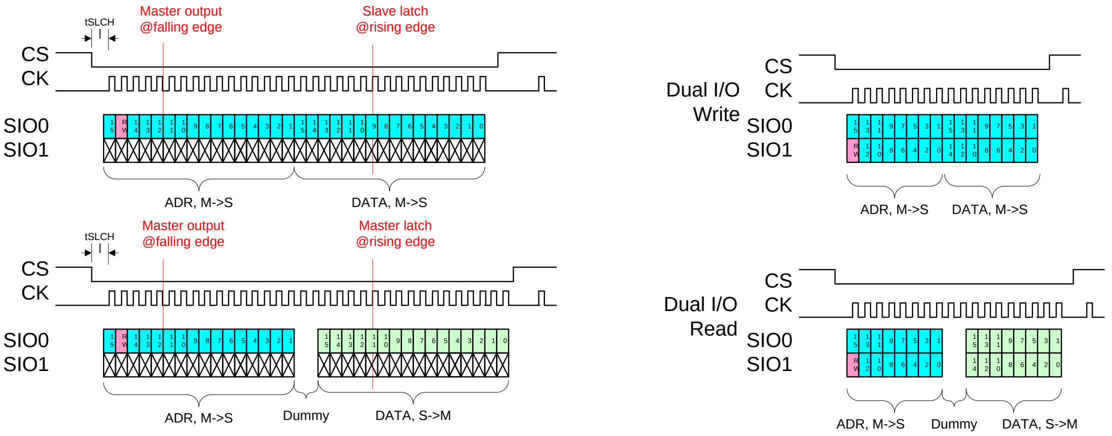
PMIC uses a 4-wire interface consisting of a clock, a chip select and two data signals (MOSI and MISO) to connect to BB. This serial-parallel interface allows BB to write commands to and read status from PMIC.

On the other hand, the IO pin (MISO) can be used as data pin or interrupt pin depending on what the system scenario is. It is used as data pin when system is in normal mode but as INT pin when system is in suspend mode.

3.2.13.1 Data Format

The pre-defined SPI format consists of two modes: Single I/O mode and dual I/O mode. Single I/O always uses MOSI as output and input. Dual I/O uses both MOSI and MISO to be output and input to achieve better channel usage. The format conveys information of R/W direction, 15-bit address (bit 15 to bit 1) and 16-bit data, and both addresses and data are MSB first. The operation waveform of SPI is illustrated as below. The SPI slave in PMIC latch data sent from the master at rising edge of clock, and output data at falling edge of clock. The parameter tSLCH, tDMMY and tCHSH are fully configurable through command registers (in BB instead of PMIC) as illustrated in the figures below.

SPI format:



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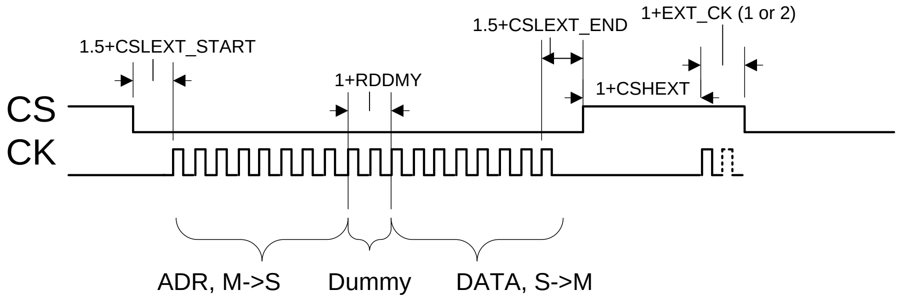
SPI parameter configuration:



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3.2.14 GPIO List

Table 3-7. MT6325 GPIO list

Pin Name	Aux Func.0	Aux Func.1	Aux Func.2	Aux Func.5	Aux Func.6	Aux Func.7	PU/PD
HOMEKEY	GPIO0	**I1:HOMEKEY**	O:INT_0	I0:TEST_CK0			**PU**/PD
SRCLKEN_IN0	GPIO1	**I1:SRCLKEN_IN0**			I0:TEST_IN0	O:TEST_OUT0	**PU**/PD
SRCLKEN_IN1	GPIO2	**I1:SRCLKEN_IN1**			I0:TEST_IN1	O:TEST_OUT1	**PU**/PD
RTC32K_1V8_0	GPIO3	**O:RTC_32K1V8_0**			I0:TEST_IN2	O:TEST_OUT2	PU/PD
RTC32K_1V8_1	GPIO4	**O:RTC_32K1V8_1**	O:INT_1	I0:TEST_CK2	I0:TEST_IN3	O:TEST_OUT3	PU/PD
SPI_CLK	GPIO5	**I0:SPI_CLK**					PU/**PD**
SPI_CSN	GPIO6	**I1:SPI_CSN**					**PU**/PD
SPI_MOSI	GPIO7	**B0:SPI_MOSI**					PU/**PD**
SPI_MISO	GPIO8	**B0:SPI_MISO**					PU/**PD**
AUD_CLK	GPIO9	**I0:AUD_CLK**		I0:TEST_CK1			PU/**PD**
AUD_DAT_MOSI	GPIO10	**I0:AUD_DAT_MOSI**	O:VOW_DAT_MISO_0		I0:TEST_IN4	O:TEST_OUT4	PU/**PD**
AUD_DAT_MISO	GPIO11	**O:AUD_DAT_MISO**	O:VOW_DAT_MISO_1		I0:TEST_IN5	O:TEST_OUT5	PU/**PD**
VOICE_CLK_MISO	GPIO12	**O:VOICE_CLK_MISO**			I0:TEST_IN6	O:TEST_OUT6	PU/**PD**
ENBB	GPIO13	**O:ENBB**			I0:TEST_IN7	O:TEST_OUT7	PU/**PD**
XOSC_EN	GPIO14	**O:XOSC_EN**					PU/**PD**

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3.3 Register Table and Descriptions

TBD

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4 Application Notes

4.1 Hardware External Shutdown

The following schematic illustrates the hardware external shut-down function for MT6325 to power down when the main chip software crashes.

- Short press PWRKEY or HOMEKEY
  - INT-> EINT -> software control
  - Power-down, sleep mode or the other functions
- Long press shut-down
  - Force power-off of PMU
  - 5/8/11/14 s with < 1% accuracy
  - External reset function with source from:
    - PWRKEY and HOMEKEY both pressed for a long period of time
      - PWRKEY and HOMEKEY do not use same key
    - PWERKEY pressed for a long period of time
    - HOMEKEY pressed for a long period of time
      - Software disables watchdog counter.

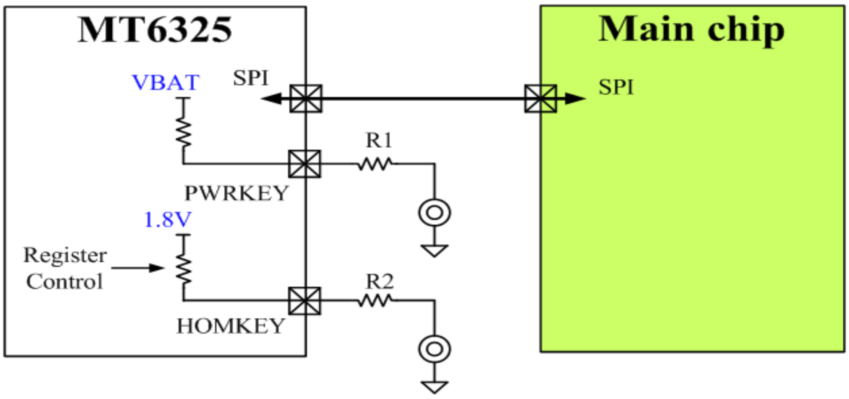

Figure 4-1. Hardware external shut-down function

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4.2 Configuration for Unused Buck Converter

The figure below shows the configuration for MT6325 VDVFS11/12, VPA and VRF18 buck converters that is not used.

- Configuration for VDVFS11/12 not in use:
  - VBAT_VDVFS11/12 connect to VBAT; GND_VDVFS11/12 connect to GND
  - VDVFS11/12: floating
  - VDVFS11/12_FB: connect to VBAT
  - GND_VDVFS11/12_FB: connect to GND
  - RG_VDVFS11_EN = 0 (software setting)
- Configuration for VPA not in use:
  - VBAT_PA connect to VBAT; GND_PA connect to GND
  - VPA & VPA_FB: floating
  - RG_VPA_EN = 0 & RG_VPA_NDIS_EN = 1 (software setting)
- Configuration for VRF18 not in use:
  - VBAT_RF18 connect to VBAT; GND_RF18 connect to GND
  - VRF18 & VRF18_FB: floating
  - RG_VRF18_EN = 0 & RG_VRF18_NDIS = 1 (software setting)

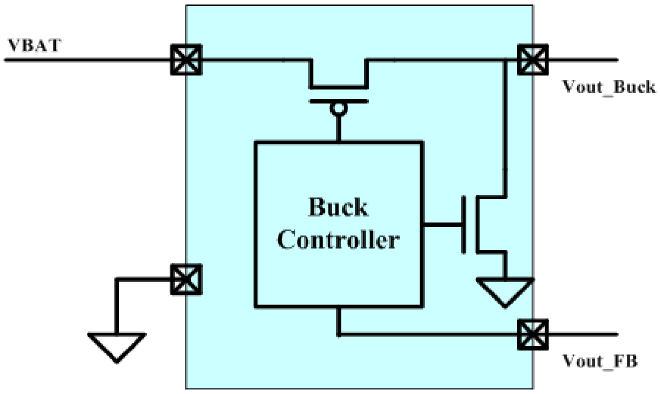

Figure 4-2. Configuration for unused DC/DC

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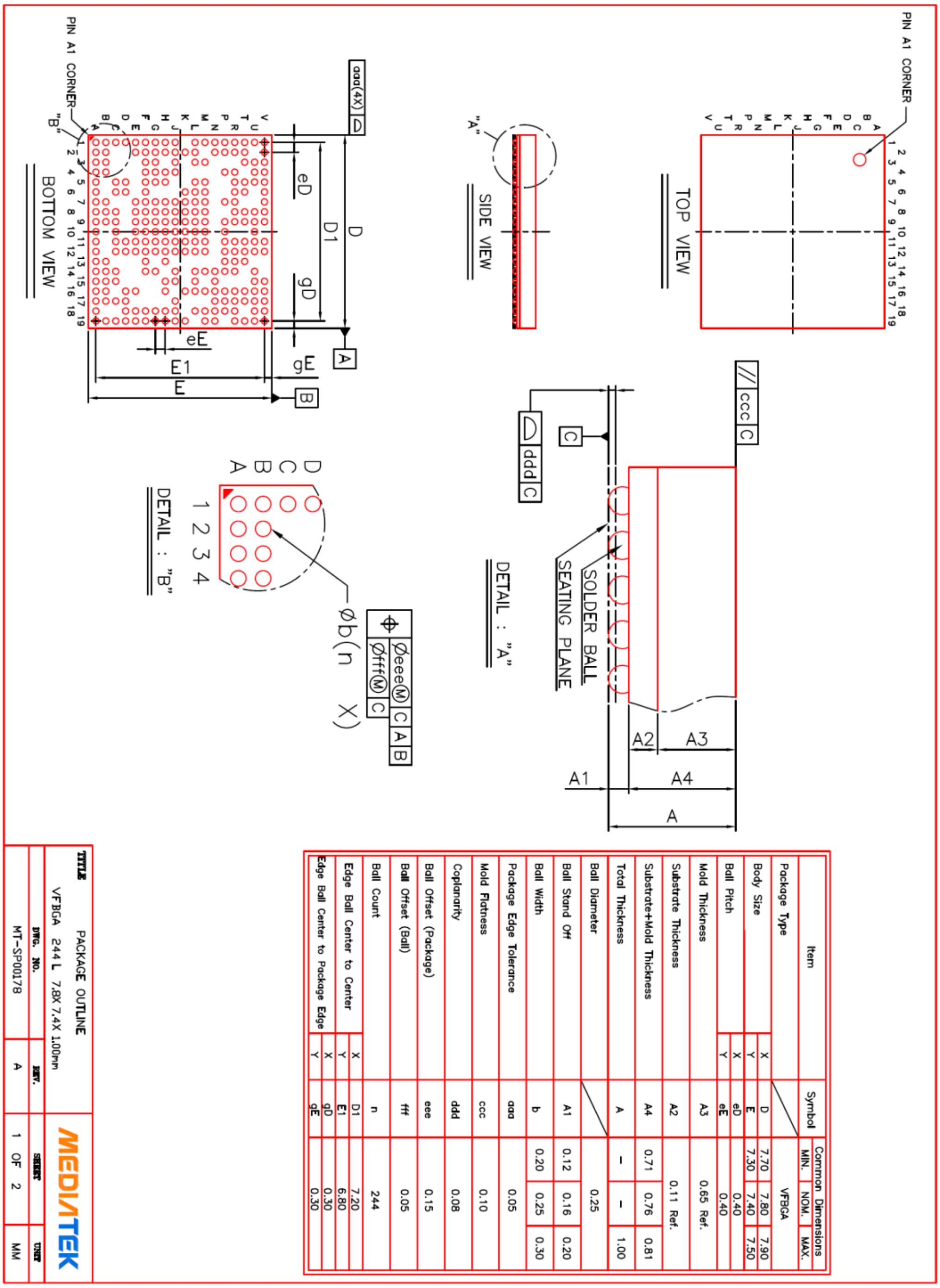
5 MT6325 Packaging

5.1 Package Dimensions



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type				VFBGA	
Body Size	X	D	7.70	7.80	7.90
	Y	E	7.30	7.40	7.50
Ball Pitch	X	eD		0.40	
	Y	eE		0.40	
Mold Thickness		A3		0.65 Ref.	
Substrate Thickness		A2		0.11 Ref.	
Substrate+Mold Thickness		A4	0.71	0.76	0.81
Total Thickness		A	–	–	1.00
Ball Diameter				0.25	
Ball Stand Off		A1	0.12	0.16	0.20
Ball Width		b	0.20	0.25	0.30
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		244	
Edge Ball Center to Center	X	D1		7.20	
	Y	E1		6.80	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

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Appendix

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